DC Voltage Controller for Asymmetric-Twin-Converter-Topology-Based High-Power STATCOM

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***Abstract*—A four-level static compensator integrating two 2-level converters, supplying/absorbing reactive power to/from the grid, is reported in our earlier paper. Reduced component count, simpler layout for switches, and smaller dc-link capacitor values are the attractive features of the proposed topology over the diode clamped and cascaded multilevel converters. This paper suggests further improvements in this topology. Suitable selection of the dc-link voltage values reduces distortion in the current fed to the grid. In addition, circuit topology is modified to avoid the split-capacitor dc links. This reduces the number of independent dc capacitor voltages to be controlled and eliminates the flow of third-harmonic current through the transformer. In order to improve the performance, a phase-shifted carrier-based pulsewidth modulation technique is used. A mathematical model of the system is derived, based on which a controller for the scheme is designed. The effectiveness of the scheme is verified through detailed simulation study. To confirm the viability of the scheme, experimental studies are carried out on a scaled-down laboratory prototype developed for the purpose.**

***Index Terms*—DC voltage regulation, harmonic suppression, multilevel operation, pulsewidth modulation (PWM), static compensator (STATCOM).**

I. Introduction

TO PROVIDE transmission-line voltage support, a static compensator (STATCOM) offers the optimal solution in terms of price, reliability, and dynamic performance [2], [3]. Generally, multipulse-converter-based [4] and multilevel-converter-based [5]–[8] solutions are used for high-power applications. A multipulse converter uses more than one voltage source converter (VSC), with common dc link, operating with nearly fundamental switching frequency, and the output of each module is connected in series through the multipulse transformer. By adjusting the triggering pulses of different VSCs, specified total harmonic distortion (THD) of the injected current is achieved with reduced switching losses as compared to that of single-VSC-based solution. The major drawback of this scheme is the high cost and complex structure of the bulky multipulse transformer.

The second solution is multilevel converters [5]–[8], which provide more than two steps in the voltages, thereby reducing THD without switching semiconductor devices at a high frequency. The two most commonly used schemes are diode clamped and cascaded converter topologies. The diode clamped multilevel topology is mostly restricted to a three-level configuration because of the complex layout of the diodes (which grows as the square of the number of levels) and the need for capacitor voltage balancing [5].

The other commonly used multilevel topology, i.e., cascaded converter topology [9]–[13], comprises several single-phase H-bridge/full-bridge converters, with separate dc links. The following are the two associated problems of this topology: 1) The size of the dc-link capacitor required is high because the instantaneous power involved with each module varies at twice the fundamental frequency [14], and 2) regulating voltage across a large number of self-supported dc-link capacitors makes the controller design complex [12], [15]–[23].

To address some of the aforementioned limitations in multilevel converters, a four-level open-ended-transformer-based multilevel converter, shown in Fig. 1, is proposed in [1]. This topology uses a reduced number of components (12 controlled switches with antiparallel diodes) as compared to the diode clamped topology (18 controlled switches with antiparallel diodes plus 18 diodes) [5]. Moreover, in this case, semiconductor switches are arranged as VSC, which enables easier structural layout and reduced driver circuit complexity. Therefore, standard VSC power modules [include six insulated-gate bipolar transistors (IGBTs) and their driver circuits in one package] can be used instead of discrete components. Moreover, this topology utilizes cascade connection of three-phase VSCs, and hence, the size of the dc-link capacitor is less as compared to that in cascaded H-bridge multilevel converter. The reduced number of dc links makes voltage regulation easier as compared to that in an equivalent cascaded converter. Comparison of diode clamped converter, cascaded converter, and open-ended transformer topologies for various parameters is given in [1].

The open-ended transformer topology has similar component layout with twin converter topology, reported in [24]. In the twin converter topology, the dc-link voltages of both VSCs are maintained equal. Therefore, only three-level operation is achieved. However, in the open-ended transformer topology, the dc-link voltage of VSC-2 is regulated to half that of VSC-1. This ensures four-level operation of the circuit [1]. Therefore, low THD is achieved with reduced filter requirements as compared to three-level twin converter topology.

Manuscript received August 29, 2011; revised December 14, 2011; accepted January 4, 2012. Date of publication January 18, 2012; date of current version September 6, 2012.

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Digital Object Identifier 10.1109/TIE.2012.2185023

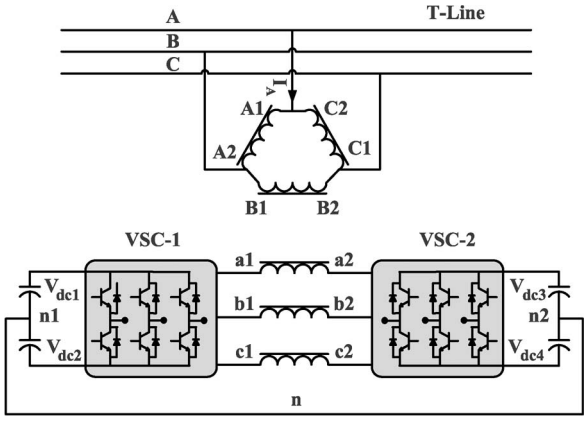

Fig. 1. Open-ended-transformer-based four-level STATCOM reported in [1].

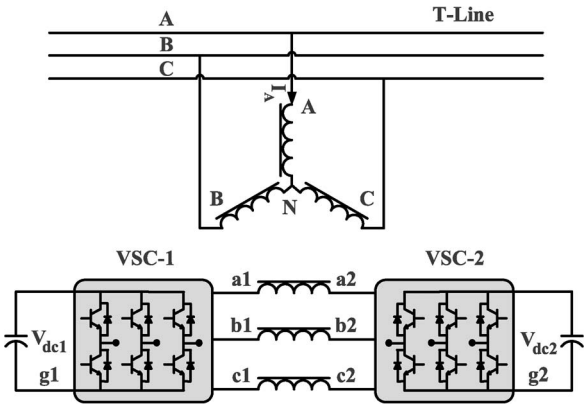

Fig. 2. Asymmetric-twin-converter-topology-based STATCOM.

A split-capacitor arrangement, used in open-ended-transformer-based circuit in [1], requires the voltage balancing of the two capacitor banks in each VSC. Therefore, a total of four dc capacitor voltages is to be regulated. This requires a complex controller and generates third-harmonic and dc currents. To address this limitation, an asymmetric twin converter topology is proposed in this paper wherein only two dc links are used without split-capacitor arrangement, as shown in Fig. 2. Furthermore, the THD of currents supplied to the grid is reduced by selecting a suitable ratio of dc-link voltages of the two VSCs. A ratio of 1:0.366 is selected based on the study of open-ended induction motor drive, which has similar power circuit configuration [25].

In this paper, the principle of operation of the proposed scheme and a suitable pulsewidth modulation (PWM) technique are discussed in Section II. Various switching states and corresponding phase voltages are provided to justify the four-level operation of the circuit. A mathematical model of the proposed topology is derived in Section III. Section IV describes the development of the controller. Operation of dc voltage regulator and reactive power controller are also discussed. The effectiveness of the proposed circuit topology and its controller are verified by detailed simulation studies provided in Section V. Viability of the proposed STATCOM is confirmed by experimental validations, and results are included in this section.

II. Proposed Multilevel Circuit Topology

A. Principle of Operation

The proposed asymmetric-twin-converter-based multilevel topology, comprising two VSCs, is shown in Fig. 2. Low-voltage (LV) windings of the transformer are connected differentially between two 2-level VSCs such that the voltage appearing on the LV side is the difference of the output voltages of two VSCs. High-voltage (HV) windings, arranged in a star configuration, are connected to the three-phase grid. Leakage inductances of the transformers act as input filter inductances of the STATCOM. Both VSCs operate with separate dc links to produce two-level individual output. Voltages appearing on the LV windings of the transformer are written in terms of output voltages of VSCs as

$$\begin{aligned} e_a &= e_{a1g1} - e_{a2g2} + e_{g1g2} \\ e_b &= e_{b1g1} - e_{b2g2} + e_{g1g2} \\ e_c &= e_{c1g1} - e_{c2g2} + e_{g1g2} \end{aligned} \tag{1}$$

where e_a, e_{a1g1}, e_{a2g2}, and e_{g1g2} are the voltages across the LV winding of phase-a, the pole voltage of VSC-1, the pole voltage of VSC-2, and the voltage difference between negative dc-link terminals of the two VSCs, respectively. Since both VSCs have separate dc links, the sum of the LV winding phase currents should be zero

$$i_a + i_b + i_c = 0. \tag{2}$$

Furthermore, the sum of instantaneous values of grid voltages is equal to zero

$$v_A + v_B + v_C = 0. \tag{3}$$

The sum of the LV winding voltages is given by

$$\begin{aligned} e_a + e_b + e_c = \frac{N_{\mathrm{LV}}}{N_{\mathrm{HV}}}(v_A + v_B + v_C) - r(i_a + i_b + i_c) \\ - L\frac{d(i_a + i_b + i_c)}{dt} \end{aligned} \tag{4}$$

where r and L are the resistance and leakage inductance as measured from the LV side, respectively, and $N_{\mathrm{LV}}/N_{\mathrm{HV}}$ is the turns ratio. Substituting (2) and (3) into (4) gives

$$e_a + e_b + e_c = 0. \tag{5}$$

Substituting LV voltages from (1) in (5) results in

$$\begin{aligned} e_{g1g2} = &-\frac{1}{3}(e_{a1g1} - e_{a2g2}) \\ &-\frac{1}{3}(e_{b1g1} - e_{b2g2}) \\ &-\frac{1}{3}(e_{c1g1} - e_{c2g2}). \end{aligned} \tag{6}$$

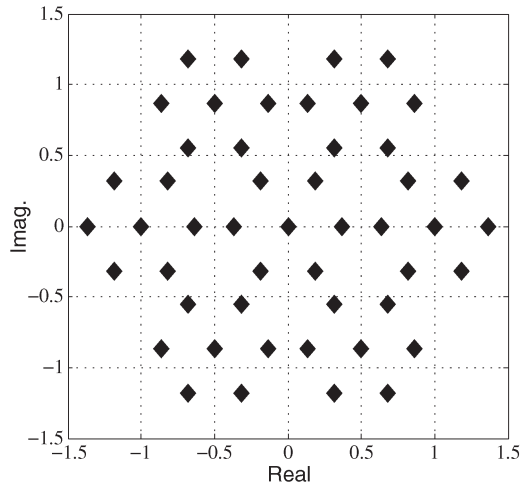

Fig. 3. Space vector diagram of 49 unique states in the proposed topology.

Substituting the value of e_{g1g2} in (1) yields

$$\begin{pmatrix} e_a \\ e_b \\ e_c \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}\begin{pmatrix} e_{a1g1} - e_{a2g2} \\ e_{b1g1} - e_{b2g2} \\ e_{c1g1} - e_{c2g2} \end{pmatrix}. \quad (7)$$

The relation between LV winding voltages and pole voltages is expressed in (7). Pole voltages depend on the conduction state of the switches in VSC-1 and VSC-2. A total of $2^6 = 64$ different combinations of states of the switches is possible. As discussed in [25], the ratio of dc-link voltages of VSCs V_{dc1} : V_{dc2} should be equal to 1:0.366 for better performance. Using this, the voltage space vector plot corresponding to unique switching states is shown in Fig. 3. Out of 64 switching states, 49 states produce unique phase voltages, and 25 voltage steps are viable in the LV-side voltage.

The line voltages of the LV side e_{ab}, e_{bc}, and e_{ca} are expressed as pole voltages using (1)

$$\begin{aligned} e_{ab} &= e_a - e_b = e_{a1g1} - e_{a2g2} - e_{b1g1} + e_{b2g2} \\ e_{bc} &= e_b - e_c = e_{b1g1} - e_{b2g2} - e_{c1g1} + e_{c2g2} \\ e_{ca} &= e_c - e_a = e_{c1g1} - e_{c2g2} - e_{a1g1} + e_{a2g2}. \end{aligned} \quad (8)$$

For $v_{\mathrm{dc2}} = 0.5v_{\mathrm{dc1}}$, depending on the state of switches, voltage waveforms of e_{ab}, e_{bc}, and e_{ca} has seven different steps. This is same as the number of steps obtained in the line voltage of four-level diode clamped multilevel converter. For $v_{\mathrm{dc2}} = 0.366v_{\mathrm{dc1}}$, nine different steps are observed in the line voltage waveforms, which is the same as that in four-level diode clamped converter with the capacitor voltage ratio $v_{\mathrm{dc1}} : v_{\mathrm{dc2}} : v_{\mathrm{dc3}}$ equal to 0.33:0.66:0.33. This makes the proposed scheme equivalent to a four-level converter.

B. PWM Strategy

LV voltage e_a takes one of the 25 values given by (7), depending on the state of the switches. The switching state is decided by the modulating waveform and the PWM strategy used. Selective harmonic elimination method (SHEM), space vector modulation (SVM), or carrier-based PWM (CB-PWM) techniques are commonly used for high-power applications. SHEM is limited in use because of its slow dynamic response. Realization of SVM for multilevel converter requires an algorithm for the identification of sector. The presence of large number of sectors makes the implementation complex [13]. Hence, the use of phase-shifted (PS) CB-PWM is suggested for the proposed topology. This PWM technique expects the controller to generate individual modulating waveforms for each inverter output e_{a1g1}, e_{b1g1}, e_{c1g1}, e_{a2g2}, e_{b2g2}, and e_{c2g2}. Each modulating waveform is compared with a carrier waveform to determine the switching state of the corresponding inverter devices. This is similar to the PS CB-PWM technique used in H-bridge cascaded converters [26], [27]. For two H-bridges per phase, the resultant waveform of ac voltages is the sum of individual converter voltages. Therefore, carrier waveforms are 180° PS from each other to cancel the carrier frequency harmonics. However, in the case of asymmetric twin converter topology, the shift in carriers is not required because the resultant waveform is the difference of two ac voltages. Comparison of modulating and carrier signals for phase-a is shown in Fig. 4. Modulated converter voltages e_{a1g1}, e_{a2g2}, and e_a for the simulated case of $V_{\mathrm{dc1}} = 805$ V, $V_{\mathrm{dc2}} = 294$ V, fundamental frequency $f = 50$ Hz, carrier frequency $fc = 900$ Hz, and modulation index $m = 0.9$ are shown in Fig. 5. The harmonic spectra of the voltage e_a are shown in Fig. 6. The absence of low-order harmonics confirms the operation of PWM technique. Dominant harmonics are present at the sideband of twice the carrier frequency. Although the sidebands of carrier frequency are also present, their magnitude is less than that of twice the carrier frequency.

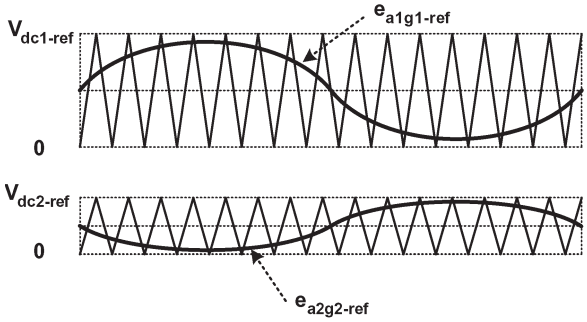

Fig. 4. Comparison of modulating and carrier waveforms for PS CB-PWM.

III. Development of the Equivalent Circuit of the System

For the purpose of analysis, an equivalent circuit of the proposed STATCOM is derived and is shown in Fig. 7. Transformer is represented by equivalent series combination of inductances, resistances, and voltage sources. To model the losses in two VSCs, two resistances r_1 and r_2 are placed in parallel to the two dc links. The governing equations of the proposed system can be derived as

$$s\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} -\frac{r\omega_b}{L} & 0 & 0 \\ 0 & -\frac{r\omega_b}{L} & 0 \\ 0 & 0 & -\frac{r\omega_b}{L} \end{pmatrix}\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + \frac{\omega_b}{L}\begin{pmatrix} -e_a + V_a \\ -e_b + V_b \\ -e_c + V_c \end{pmatrix} \quad (9)$$

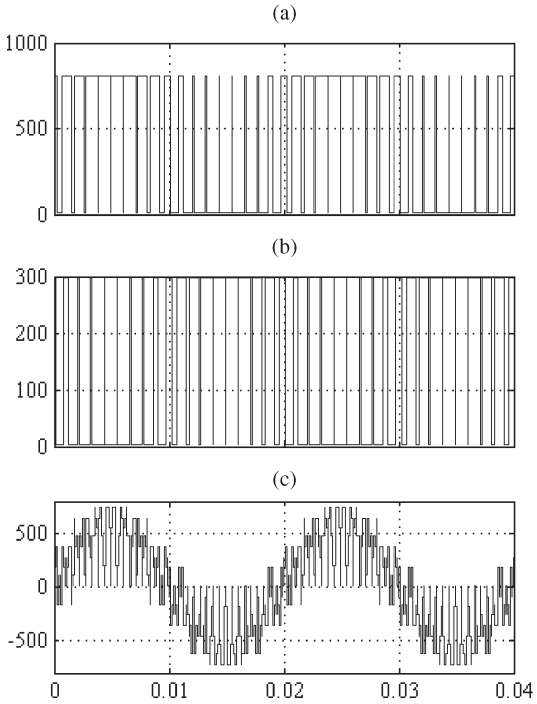

Fig. 5. Simulated voltage waveforms. (a) Pole voltage e_{a1g1}. (b) Pole voltage e_{a2g2}. (c) LV-side voltage e_a. (X-axis) Time (in seconds).

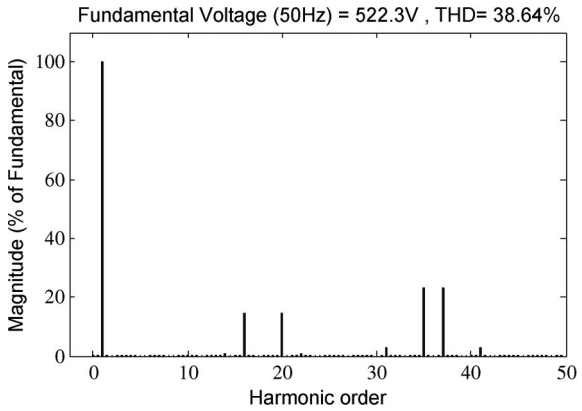

Fig. 6. Harmonic spectrum of LV-side voltage e_a.

where L is defined as $\omega_b l/z_{\rm base}$. l, ω_b, and $z_{\rm base}$ are the leakage inductance, base frequency, and base impedance of STATCOM. All the parameters and variables are expressed in per-unit (p.u.) system. Equation (9) is transformed into $dq0$ reference frame, which has been defined in the Appendix. The system variables in the $dq0$ frame are expressed as follows:

$$s\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} -\frac{r\omega_b}{L} & \omega \\ -\omega & -\frac{r\omega_b}{L} \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix} + \frac{\omega_b}{L}\begin{pmatrix} -e_{d1}+e_{d2}+|V| \\ -e_{q1}+e_{q2} \end{pmatrix} \tag{10}$$

where i_d and i_q are the d- and q-axis components of LV-side currents. e_{d1} and e_{q1} are the voltage components of VSC-1, and e_{d2} and e_{q2} are the voltage components of VSC-2. Equation (10) interrelates the ac parameters of the STATCOM with those of the grid. The dependence between dc and ac parameters of STATCOM is derived using instantaneous power balance equations. The following equation gives the power balance condition between the ac and dc links of VSC-1:

$$v_{\rm dc1} i_{\rm dc1} = \frac{3}{2}(e_{d1} i_d + e_{q1} i_q). \tag{11}$$

The current flowing through the dc-link capacitor c_1 is related to the dc-link voltage $v_{\rm dc1}$ as follows:

$$s v_{\rm dc1} = \omega_b C_1 \left(i_{\rm dc1} - \frac{v_{\rm dc1}}{r_1} \right) \tag{12}$$

where C_1 is defined as $1/(\omega_b c_1 z_{\rm base})$. Substituting $i_{\rm dc1}$ from (11)

$$s v_{\rm dc1} = \omega_b C_1 \left(\frac{3}{2v_{\rm dc1}}(e_{d1} i_d + e_{q1} i_q) - \frac{v_{\rm dc1}}{r_1} \right). \tag{13}$$

Similarly, the governing equation for VSC-2 is expressed as

$$s v_{\rm dc2} = \omega_b C_2 \left(\frac{-3}{2v_{\rm dc2}}(e_{d2} i_d + e_{q2} i_q) - \frac{v_{\rm dc2}}{r_2} \right). \tag{14}$$

Equations (10), (13), and (14) represent the behavior of the system. These equations are used in the following section.

IV. Development of the Controller

The proposed asymmetric-twin-converter-based STATCOM has two dc-link voltages $v_{\rm dc1}$ and $v_{\rm dc2}$. The controller should regulate these two dc-link voltages and govern the total reactive power flowing to/from the STATCOM. The total active power required to overcome losses and regulate dc-link voltages is drawn by STATCOM from the grid. This active power needs to be redistributed among the two dc links. The distribution should ensure that the two dc-link voltages $v_{\rm dc1}$ and $v_{\rm dc2}$ are maintained equal to their corresponding reference values. The suitable controller to achieve these objectives is discussed in this section.

A. Current Control

The overall system is represented by two coupled differential equations, as depicted in (10). To decouple them, two variables x_1 and x_2 are defined such that

$$-e_{d1} + e_{d2} = \frac{L}{\omega_b}(x_1 - \omega i_q) - |V| \tag{15}$$

$$-e_{q1} + e_{q2} = \frac{L}{\omega_b}(x_2 + \omega i_d). \tag{16}$$

By combining (10) with (15) and (16), the decoupled system equations are obtained as follows:

$$s\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} -\frac{r\omega_b}{L} & 0 \\ 0 & -\frac{r\omega_b}{L} \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix} + \frac{\omega_b}{L}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix}. \tag{17}$$

Applying small-signal analysis on the decoupled system of (17), the small-signal plant transfer function is derived as

$$G(s) = \frac{\Delta i_d}{\Delta x_1} = \frac{\Delta i_q}{\Delta x_2} = \frac{1}{s + \frac{r\omega_b}{L}}. \tag{18}$$

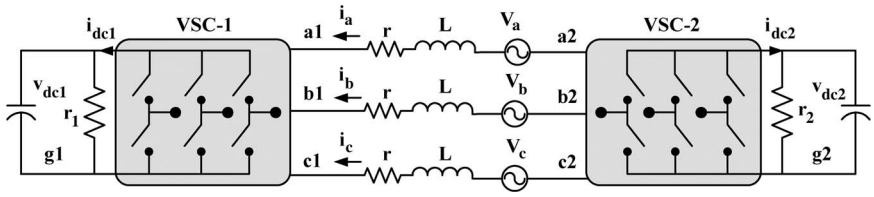

Fig. 7. Equivalent circuit diagram of the proposed STATCOM.

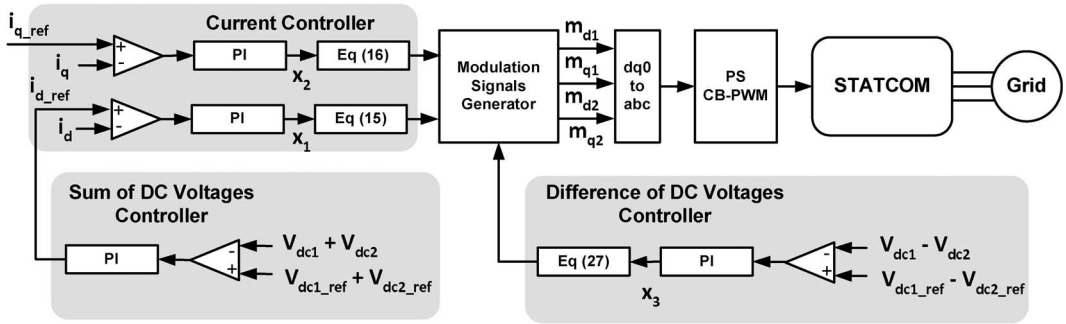

Fig. 8. Controller for STATCOM.

Control variables x_1 and x_2 govern the system currents i_d and i_q, respectively, as per the differential equation (17). Therefore, current control is achieved by controlling variables x_1 and x_2 using the errors between reference values and actual currents, as given by

$$x_1 = k_{p1}(i_{d\_\mathrm{ref}} - i_d) + k_{i1}\int (i_{d\_\mathrm{ref}} - i_d)\,dt \qquad (19)$$

$$x_2 = k_{p2}(i_{q\_\mathrm{ref}} - i_q) + k_{i2}\int (i_{q\_\mathrm{ref}} - i_q)\,dt. \qquad (20)$$

Required LV voltages $e_{d1} - e_{d2}$ and $e_{q1} - e_{q2}$ are derived by using these values of x_1 and x_2 in (15) and (16). To generate these voltages, modulation signals for the VSCs are derived as follows:

$$m_{d1} = \frac{e_{d1}}{v_{\mathrm{dc1}}}; m_{q1} = \frac{e_{q1}}{v_{\mathrm{dc1}}}; m_{d2} = \frac{e_{d2}}{v_{\mathrm{dc2}}}; m_{q2} = \frac{e_{q2}}{v_{\mathrm{dc2}}}. \qquad (21)$$

An inner current controller is implemented using (15), (16), and (19)–(21), as shown in Fig. 8.

The inner current controller generates the modulating waveforms of LV voltages ($m_{d1}v_{\mathrm{dc1}} - m_{d2}v_{\mathrm{dc2}}$) and ($m_{q1}v_{\mathrm{dc1}} - m_{q2}v_{\mathrm{dc2}}$). However, modulating waveforms for individual VSCs m_{d1}, m_{d2}, m_{q1}, and m_{q2} have to be derived from these LV voltages. This distribution is used to regulate real power exchange between the two VSCs, as given in Section IV-C.

Furthermore, the current controller requires the reference current signals i_{d_ref} and i_{q_ref} as inputs. The phase-locked loop is synchronized with the grid voltage such that q component of the grid voltage is kept equal to zero. Therefore, the total active and reactive powers absorbed or supplied by the STATCOM are proportional to i_{d_ref} and i_{q_ref}, respectively. The outer cascaded controller generates the reference current signals i_{d_ref} and i_{q_ref} such that the system variables (total reactive power and two dc-link voltages) are maintained at their respective reference values.

B. Reactive Power Control

STATCOMs are commonly used either for transmission-line voltage support or for reactive power compensation of load. For voltage support of the transmission line, the reactive current reference i_{q_ref} is controlled by the deviation of the transmission-line voltage from its nominal value. On the other hand, for load compensation operation, the reactive current reference i_{q_ref} is controlled by the deviation of source power factor from its required value. In both the aforementioned cases, i_{q_ref} will be supplied to the current controller by a higher level controller. The issues pertaining to the higher level controller are kept outside the purview of this paper.

C. DC Voltage Control

A dc voltage controller should ensure that the two dc-link voltages v_{dc1} and v_{dc2} are regulated at their reference values. This problem is divided into two separate control objectives: first, to maintain the sum of two dc-link voltages ($v_{\mathrm{dc1}} + v_{\mathrm{dc2}}$) that is equal to the sum of their reference values ($v_{\mathrm{dc1-ref}} + v_{\mathrm{dc2-ref}}$) and, second, to maintain the difference of the two dc-link voltages ($v_{\mathrm{dc1}} - v_{\mathrm{dc2}}$) that is equal to the difference of their reference values ($v_{\mathrm{dc1-ref}} - v_{\mathrm{dc2-ref}}$).

1) Sum of DC Voltages: The sum of the dc voltages ($v_{\mathrm{dc1}} + v_{\mathrm{dc2}}$) increases with the net real power flow from grid to STATCOM and vice versa. In other words, the error in the sum of dc-link voltages ($v_{\mathrm{dc1}} + v_{\mathrm{dc2}} - v_{\mathrm{dc1-ref}} - v_{\mathrm{dc2-ref}}$) indicates the amount of real power to be absorbed from the grid. Hence, the d-axis reference current i_{d_ref} is controlled by the error existing between reference and actual dc-link voltages of VSCs, as shown in Fig. 8.

2) Difference of DC Voltages: System equations (13) and (14) are coupled equations describing the behavior of the dc-link voltages. Considering $C_1 = C_2 = C$ and subtracting (14) from (13) give

$$s(v_{\mathrm{dc1}} - v_{\mathrm{dc2}}) = x_3 - \omega_b C\left(\frac{v_{\mathrm{dc1}}}{r_1} - \frac{v_{\mathrm{dc2}}}{r_2}\right) \qquad (22)$$

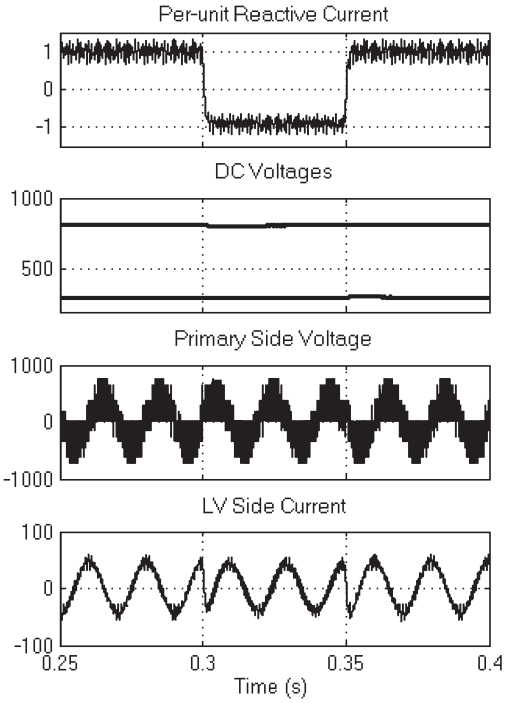

Fig. 9. Simulated transient test results. (i) p.u. reactive current i_q. (ii) DC-link voltages $v_{\rm dc1}$ and $v_{\rm dc2}$. (iii) LV-side voltage e_a. (iv) LV-side phase-a transformer current i_a.

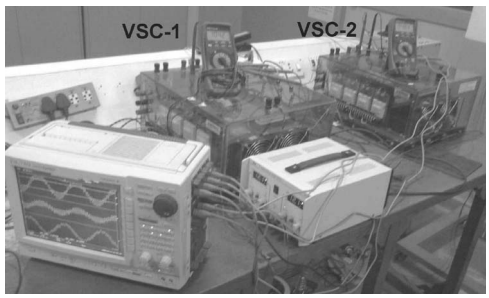

Fig. 10. Scaled-down laboratory prototype of STATCOM.

TABLE I
CIRCUIT PARAMETERS OF EXPERIMENTAL PROTOTYPE

Parameter	Value
Power Rating	2.3kVA
Power Frequency	50Hz
LV side voltage, e_a	107Vrms
Switching Frequency	900Hz
DC link voltage, v_{dc1}	282V
DC link voltage, v_{dc2}	106V
DC link capacitor, C	825μF
Leakage inductance, L	2.1mH

where

$$x_3 = \frac{3\omega_b C}{2}\left[i_d\left(\frac{e_{d1}}{v_{\rm dc1}}+\frac{e_{d2}}{v_{\rm dc2}}\right)+i_q\left(\frac{e_{q1}}{v_{\rm dc1}}+\frac{e_{q2}}{v_{\rm dc2}}\right)\right]. \tag{23}$$

Substituting modulation signals from (21) into (23) gives

$$x_3 = \frac{3\omega_b C}{2}\left[i_d(m_{d1}+m_{d2})+i_q(m_{q1}+m_{q2})\right] \tag{24}$$

$$x_3 = \frac{3\omega_b C}{2}(\overrightarrow{m}\bullet\overrightarrow{i}) \tag{25}$$

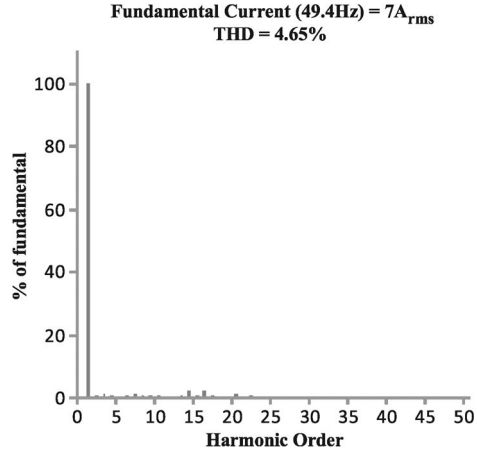

Fig. 11. Experimentally obtained harmonic spectrum of phase-a current.

where the modulation vector $\overrightarrow{m} = m_{d1}+m_{d2}+j(m_{q1}+m_{q2})$ and the current vector $\overrightarrow{i} = i_d + ji_q$. Considering $r_1 = r_2 = r$ and applying small-signal analysis on (22) give the transfer function

$$H(s) = \frac{\Delta v_{\rm dc1}-\Delta v_{\rm dc2}}{\Delta x_3} = \frac{1}{s+\frac{\omega_b C}{r}}. \tag{26}$$

Equation (22) gives the relation between the control variable x_3 and the difference of dc-link voltages $v_{\rm dc1}-v_{\rm dc2}$. Therefore, it is inferred that error $(v_{\rm dc1\_ref}-v_{\rm dc2\_ref})-(v_{\rm dc1}-v_{\rm dc2})$ is to be processed through a proportional–integral controller to obtain the control variable x_3. Hence, the difference in power requirement between VSC-1 and VSC-2 is reflected in x_3. Using it, $(\overrightarrow{m}\bullet\overrightarrow{i})$ is determined from (25). To achieve the required power flow between VSCs with low dc-link voltages, the modulation vector $\overrightarrow{m}$ is maintained in phase with $\overrightarrow{i}$. Hence

$$|\overrightarrow{m}| = \frac{2}{3\omega_b C|\overrightarrow{i}|}x_3, \qquad \angle\overrightarrow{\Delta m} = \angle\overrightarrow{i}. \tag{27}$$

The controller which ensures that the difference of dc voltages $v_{\rm dc1}-v_{\rm dc2}$ is maintained equal to the reference $v_{\rm dc1\_ref}-v_{\rm dc2\_ref}$ is shown in Fig. 8.

D. Generation of Modulation Signals

The current controller, shown in Fig. 8, generates the signals for primary voltages $e_{d1}-e_{d2}$ and $e_{q1}-e_{q2}$. These are transformed to modulation signals as follows:

$$\begin{aligned} m_{d1}v_{\rm dc1}-m_{d2}v_{\rm dc2} &= e_{d1}-e_{d2} \\ m_{q1}v_{\rm dc1}-m_{q2}v_{\rm dc2} &= e_{q1}-e_{q2}. \end{aligned} \tag{28}$$

Furthermore, the "Difference of DC Voltages" controller generates $m_{d1}+m_{d2}$ and $m_{q1}+m_{q2}$. By arithmetic operation on the outputs of these two controllers, the individual modulation signals for the two VSCs m_{d1}, m_{q1}, m_{d2}, and m_{q2} are generated by the block "Modulation Signals Generator," as shown in Fig. 8. These signals are then converted to stationary abc frame of reference. The modulation waveforms for the two

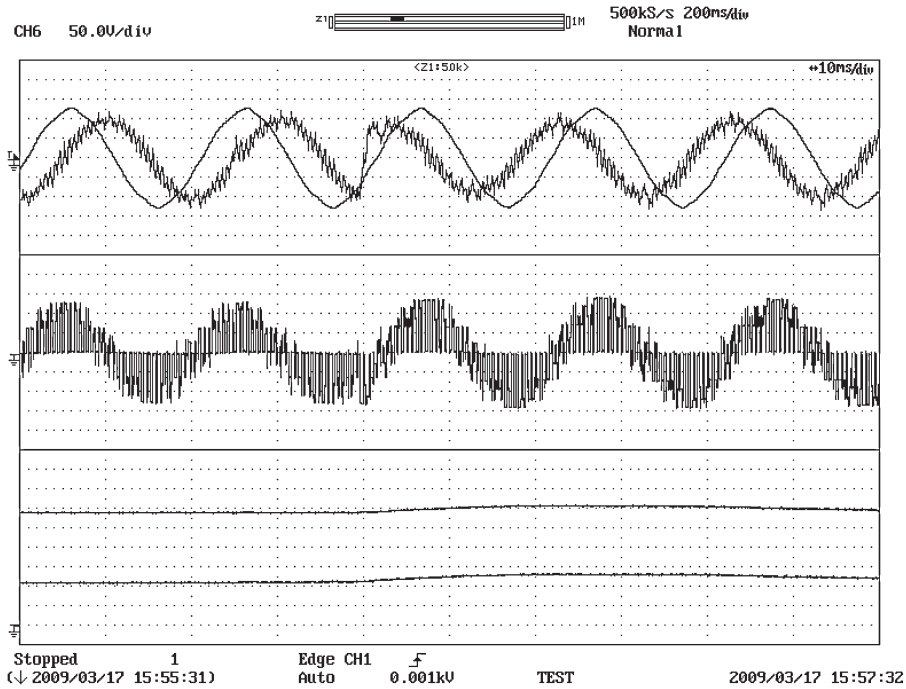

Fig. 12. Experimentally obtained transient response of the proposed scheme (X-axis: 10 ms/div). (i) HV-side (grid) phase-a voltage v_A (200 V/div) and LV-side phase-a transformer current i_a (5 A/div). (ii) LV-side voltage e_a (100 V/div). (iii) DC-link voltages $v_{\rm dc1}$ and $v_{\rm dc2}$ (50 VA/div).

VSCs are then compared with the carrier waveforms to generate gating signals for VSCs.

V. Results and Discussion

A. Simulation Studies

In order to verify the efficacy of the proposed scheme, a 50-kVA asymmetric-twin-converter-based STATCOM has been simulated on MATLAB/Simulink platform utilizing the following parameters: phase voltage at LV side $e_a = 370$ Vrms, leakage inductance $L = 0.14$ p.u., dc capacitor $C = 4700$ μF, switching frequency $f_s = 900$ Hz, and dc-link voltages $v_{\rm dc1} = 805.2$ V and $v_{\rm dc2} = 294.7$ V. In order to evaluate the performance of the scheme, step changes in reactive current reference $i_{q\_{\rm ref}}$ from $+1$ p.u. (capacitive) to -1 p.u. (inductive) and from -1 p.u. to $+1$ p.u. are initiated at 0.3 and 0.35 s, respectively. The performance of the scheme for the aforementioned cases is shown in Fig. 9. The p.u. reactive current i_q, dc-link voltages $v_{\rm dc1}$ and $v_{\rm dc2}$, LV-side voltage e_a, and LV-side phase-a current i_a are shown in Fig. 9(i)–(iv), respectively. Stable operation of the system for large change in the reactive current demonstrates the robustness of the controller. Regulation of dc-link voltages at their reference values ensures that the proposed dc voltage controller is effective both during steady-state and transient conditions.

B. Experimental Setup

To confirm the viability of the scheme, experimental studies are carried out utilizing a scaled-down laboratory prototype developed for the purpose. A prototype including VSCs and the measuring instruments are shown Fig. 10. A digital signal processor TM.S.320F2812 is used to implement the control laws derived in the previous section. PWM signals for VSC-1 and VSC-2 are generated using event manager modules A and B of TM.S.320F2812, respectively. SKHI-22A drivers are used to generate gate signals for IGBT modules. Various circuit parameters of the prototype are given in Table I.

The harmonic spectrum of phase-a LV-side current i_a is shown in Fig. 11. At full-load steady-state operation in capacitive mode, THD is observed to be 4.65%. The fifth and seventh harmonic components of current are found to be 0.33% and 1.2% of the fundamental, respectively. Low distortion in current confirms the usability of the circuit for HV transmission lines.

In order to evaluate the transient performance of the scheme, a step change of -1 p.u. (inductive) to $+1$ p.u. (capacitive) is initiated in p.u. reactive current reference $i_{q\_{\rm ref}}$. The transient performance of the scheme for the aforementioned cases is shown in Fig. 12. HV-side (grid) phase-a voltage v_A and LV-side current i_a, LV-side voltage e_a, and dc-link voltages $v_{\rm dc1}$ and $v_{\rm dc2}$ are shown in Fig. 12(i)–(iii), respectively. As observed, the phase current lags voltage by 4.5 ms (80°), which confirms the inductive mode operation of the STATCOM. After the step change in reactive current reference, the phase current leads voltage by 80°, which confirms capacitive mode. Changeover from rated current in inductive mode to that in capacitive mode is achieved within 5 ms (quarter of a cycle), from which it can be inferred that the system response is quite fast. Less than 8% overshoot in dc voltages over the steady-state value is observed. Moreover, the phase current does not depict any overshoot and maintains low THD even after the step change. These observations elucidate a good transient and steady-state performance of the proposed STATCOM.

VI. Conclusion

A high-power STATCOM based on two 2-level VSCs is reported in [1]. Reduced component count, simpler layout of switches, and reduced capacitance requirement are the attractive features of the scheme over the diode clamped and cascaded multilevel converters. In this paper, an effort has been made to improve the performance of open-ended transformer topology presented in [1]. In the proposed topology, only two dc voltages have to be controlled. Furthermore, the ratio of the dc-link voltages of the two VSCs is selected such that low distortion in current is achieved. A dc-link voltage controller has been proposed to regulate the dc-link voltages of the two converters by drawing requisite amount of real power from the utility and by differentially distributing them between the two converters. A mathematical model of the system is developed to facilitate the design of the controller. Detailed simulation studies are carried out to verify the efficacy of the scheme. In order to confirm the viability of the scheme, experimental studies are carried out utilizing a scaled-down laboratory prototype developed for the purpose.

Appendix
Synchronously Rotating $dq0$ Frame

$$\begin{pmatrix} d \\ q \\ 0 \end{pmatrix} = \frac{2}{3} \begin{pmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \times \begin{pmatrix} a \\ b \\ c \end{pmatrix}. \quad (29)$$

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