JPE 13-3-8

http://dx.doi.org/10.6113/JPE.2013.13.3.400

A Discrete State-Space Control Scheme for Dynamic Voltage Restorers

He Lei[†], Xin-Chun Lin[*], Ming-Yu Xue[*], and Yong Kang[*]

[†*]College of Electrical and Electronic Engineering, State Key Laboratory of Advanced Electromagnetic Engineering and Technology, Huazhong University of Science and Technology, Wuhan, China

Abstract

This paper presents a discrete state-space controller using state feedback control and feed-forward decoupling to provide a desirable control bandwidth and control stability for dynamic voltage restorers (DVR). The paper initially discusses three typical applications of a DVR. The load-side capacitor DVR topology is preferred because of its better filtering capability. The proposed DVR controller offers almost full controllability because of the multi-feedback of state variables, including one-beat delay feedback. Feed-forward decoupling is usually employed to prevent disturbances of the load current and source voltage. Directly obtaining the feed-forward paths of the load current and source voltage in the discrete domain is a complicated process. Fortunately, the full feed-forward decoupling strategy can be easily applied to the discrete state-space controller by means of continuous transformation. Simulation and experimental results from a digital signal processor-based system are included to support theoretical analysis.

Key words: Dynamic voltage restorer, Feed-forward decoupling, One-beat delay, State feedback control

I. INTRODUCTION

Voltage sags have become one of the most important power quality problems in recent years because of the extensive use of voltage-sensitive loads including computers, adjustable speed drives, and programmable logic controllers [1]. Voltage sags are defined as sudden voltage drops (between 10% and 90% of the nominal voltage) lasting for a few cycles. They are mainly caused by short circuits and starting large motors.

The application of dynamic voltage restorers (DVR) has attracted much attention because a DVR system is one of the most efficient devices for mitigating voltage sags [2]-[4]. A DVR injects a compensation voltage in series with the source voltage to stabilize the load voltage. Moreover, a DVR can function like a virtual line impedance that limits the line fault current of a downstream fault [5]-[7].

A typical DVR topology is composed of an energy storage device, a voltage source inverter, an LC filter, and an injection transformer for the series connection. Fig. 1 presents three typical DVR topologies, which are classified by the filter capacitor position [8]. Fig. 1(a) shows a filter capacitor that is placed on the converter side of the transformer, which will be referred as topology "a." As a result of the leakage inductance of the transformer, the filter inductor can be omitted, and the filter capacitor can be placed on the utility side of the transformer Fig. 1(b), which will be referred as topology "b." The filter capacitor can also be placed on the load side of the transformer parallel to the load Fig. 1(c), which will be referred as topology "c."

From the perspective of the control object, the control methods of a DVR can be essentially classified into direct control and indirect control. For direct control, the control object is the load voltage. For indirect control, the control object is the compensation voltage. The open-loop transfer function is the same for both controls. The source voltage is considered as a disturbance for direct control, whereas the source voltage is part of the reference for indirect control. With regard to the load-side capacitor DVR topology, direct control is preferred.

Compensating the load voltage to its reference value is desirable for a DVR. The reference value should be unaffected by voltage sags. Various control methods for a DVR have been proposed in previous studies [9]-[19], including proportional resonant control [9], [10], state feedback control [11], [12], repetitive control [13], [14], H∞ control [15], [16], predictive control [17], etc. Several active damping methods

Manuscript received Nov. 20, 2012; revised Feb. 1, 2013
Recommended for publication by Associate Editor Jun-Keun Ji.
[†]Corresponding Author: regallyhust@yahoo.cn
Tel: +86-27-87541114, Fax: +86-27-87545438, Huazhong University of Science and Technology
[*]College of Electrical and Electronic Engineering, State Key Laboratory of Advanced Electromagnetic Engineering and Technology, Huazhong University of Science and Technology, China

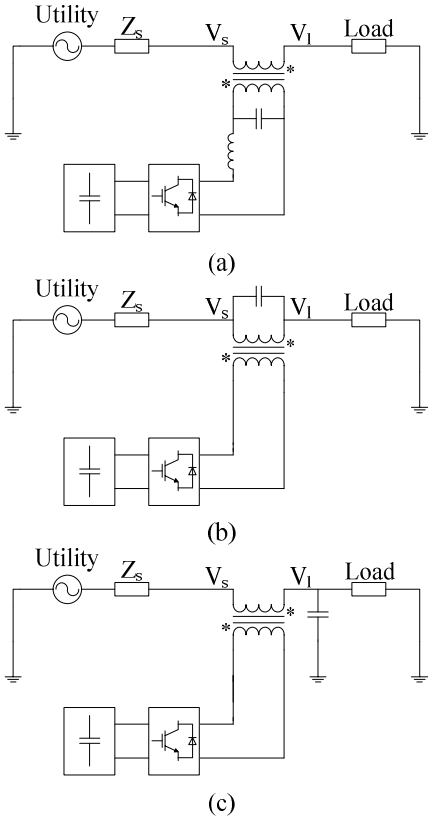


Fig. 1. Three typical applications of a DVR: (a) Filter capacitor placed on the converter side, (b) filter capacitor placed on the utility side, and (c) filter capacitor placed on the load side.

can be combined with the classic control method to damp the LC resonance, such as a virtual resistor and the Posicast controller [18], [19]. From the pole perspective, the performance of the control system relies on appropriate pole placement. A single-loop control method with direct pole placement was proposed in [20]. However, the closed-loop natural frequency cannot be designed directly because of the lack of freedom degrees, which has an effect on the control bandwidth.

This paper proposes a simple but effective control system for the load-side capacitor DVR topology based on the discrete state-space technique. A one-beat delay (OBD) exists in practical digital control systems, which can be sent as feedback as an extra state variable. Therefore, the poles and zero of the control system can be placed directly according to the desired closed-loop natural frequency and damping ratio because of sufficient freedom degrees. The aforementioned control variables can be simply calculated using the formulas presented in this paper. For direct control, the load current and source voltage are both disturbances in the control system. Thus feed-forward decoupling is adopted for rejecting disturbances because of its simplicity and effectiveness. The feed-forward paths of the load current and source voltage are obtained in the continuous domain. Then

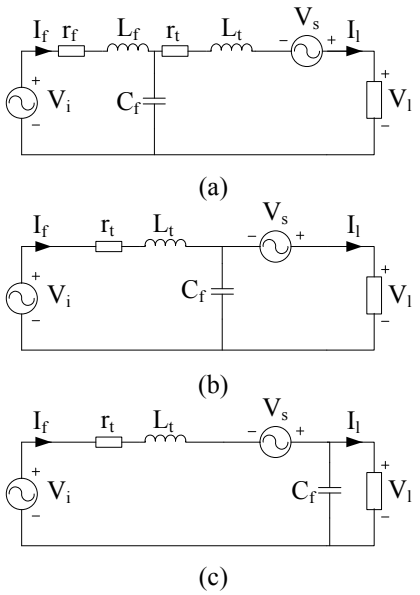


Fig. 2. Single-phase equivalent circuit of the three topologies: (a) Topology "a," (b) topology "b," and (c) topology "c."

they are discretized and implemented in the digital controller. Simulation and experimental results demonstrate the efficacy of the proposed control strategy.

II. TOPOLOGY ANALYSIS

The respective single-phase equivalent circuits are shown in Fig. 2 according to the three typical applications of the DVR in Fig. 1. V_i, V_s, and V_l are the inverter output voltage, source voltage, and load voltage, respectively. I_f and I_l are the filter inductor current and load current, respectively. L_f, r_f, and C_f are the filter inductance, parasitic resistance, and filter capacitance, respectively. L_t and r_t are the leakage inductance and winding resistance of the injection transformer, respectively. The turn ratio of the injection transformer is assumed to be 1:1.

The reference of the inverter output voltage is given as

$$V_i^* = V_l^* - V_s . \quad (1)$$

where V_l^* is the reference of the load voltage. Considering that the time delay occurs in a digital control system, the inverter voltage can be expressed as

$$V_i = V_i^* * e^{-sT_d} . \quad (2)$$

The system delay (T_d) can be modeled as the sum of the one sampling period delay (T_s) and the zero-order hold delay ($0.5 * T_s$) [11].

Therefore, the load voltage for the open-loop control configuration can be written as

$$V_l = G_{vl\_vr\_n}(s) * V_l^* + G_{vl\_il\_n}(s) * I_l + G_{vl\_vs\_n}(s) * V_s \,. \quad (3)$$

where n = a, b, c, which stand for the three DVR topologies. $G_{vl\_vr\_n}(s)$ is the open-loop transfer function from the load reference voltage to the load voltage; $G_{vl\_il\_n}(s)$ is the open-loop transfer function from the load current to the load voltage; and $G_{vl\_vs\_n}(s)$ is the open-loop transfer function from the source voltage to the load voltage. These transfer functions are defined as

$$G_{vl\_vr\_a}(s) = G_{vl\_vr\_b}(s) = G_{vl\_vr\_c}(s) = \frac{1}{\left(s^2 L_{f/t} C_f + s r_{f/t} C_f + 1\right) e^{sT_d}} \,, \quad (4)$$

$$G_{vl\_il\_a}(s) = \frac{\left(s^2 L_t C_f + s r_t C_f\right)\left(sL_f + r_f\right) + sL_f + sL_t + r_f + r_t}{\left(s^2 L_f C_f + s r_f C_f + 1\right)} \,, \quad (5)$$

$$G_{vl\_il\_b}(s) = G_{vl\_il\_c}(s) = \frac{sL_t + r_t}{\left(s^2 L_t C_f + s r_t C_f + 1\right)} \,, \quad (6)$$

$$G_{vl\_vs\_a}(s) = G_{vl\_vs\_b}(s) = \frac{\left(s^2 L_{f/t} C_f + s r_{f/t} C_f + 1\right) e^{sT_d} - 1}{\left(s^2 L_{f/t} C_f + s r_{f/t} C_f + 1\right) e^{sT_d}} \,, \text{ and} \quad (7)$$

$$G_{vl\_vs\_c}(s) = \frac{e^{sT_d} - 1}{\left(s^2 L_t C_f + s r_t C_f + 1\right) e^{sT_d}} \,. \quad (8)$$

Equations (4) to (8) show that discrepancies among the three DVR topologies are caused by disturbances of the load current and source voltage. Fig. 3 illustrates a bode diagram of $G_{vl\_il\_n}(s)$, and Fig. 4 illustrates a bode diagram of $G_{vl\_vs\_n}(s)$. A non-integer sample of e^{sT_d} is difficult to realize. As a result, the Taylor-expansion is employed hereafter.

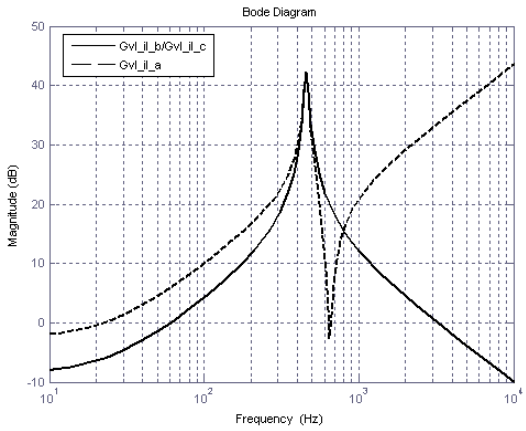


Fig. 3. Bode diagram of the open-loop transfer function from load current to load voltage for the three topologies.

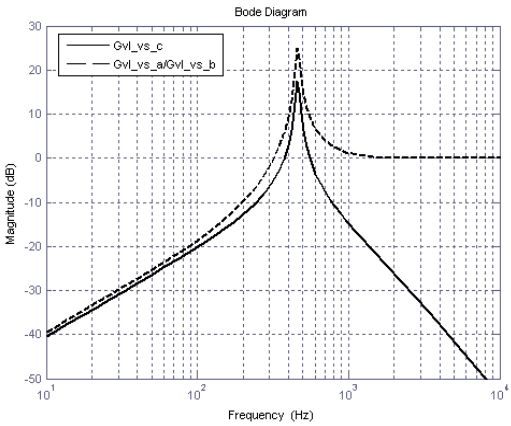


Fig. 4. Bode diagram of the open-loop transfer function from source voltage to load voltage for the three topologies.

With regard to topology "a," the load voltage may not achieve its desired reference value because of the extra voltage drop across the leakage impedance of the injection transformer. However, topologies "b" and "c" will not encounter this problem. Based on Fig. 3, a conclusion can be drawn that topologies "b" and "c" have better capabilities of rejecting load current disturbances when compared with topology "a."

With regard to topology "c," the source voltage can be filtered by an LC circuit. Fig. 4 shows that a high-frequency source voltage disturbance can be attenuated. In other words, topology "c" has better capability of rejecting source voltage disturbances when compared with topologies "a" and "b." Therefore, topology "c" is recommended in this study.

III. Discrete State-Space Controller

A. System Modeling

Based on Fig. 2(c), by applying Kirchhoff's voltage and current laws, the following equations can be derived as

$$\begin{aligned} V_i &= V_l - V_s + r_t I_t + L_t \frac{dI_f}{dt} \\ I_f &= C_f \frac{dV_l}{dt} + I_l \end{aligned} \,. \quad (9)$$

Equation (9) can be written in state-space form as

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \,, \quad (10)$$

where

$$x = \begin{bmatrix} V_l & I_f \end{bmatrix}^T, \qquad u = \begin{bmatrix} V_i & I_l & V_s \end{bmatrix}^T,$$

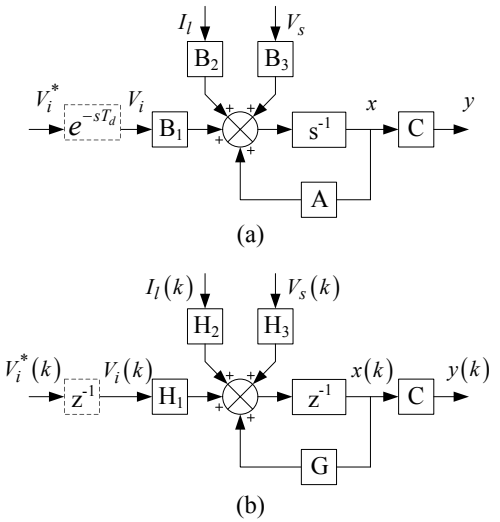


Fig. 5. State-space model of a single-phase DVR of topology "c" in (a) continuous domain and (b) discrete domain.

$$A=\begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_t} & -\frac{r_t}{L_t} \end{bmatrix},\quad B=\begin{bmatrix} B_1 \mid B_2 \mid B_3 \end{bmatrix}=\begin{bmatrix} 0 & -\frac{1}{C_f} & 0 \\ \frac{1}{L_t} & 0 & \frac{1}{L_t} \end{bmatrix},$$

$$C=\begin{bmatrix} 1 & 0 \end{bmatrix}.$$

Equation (10) can be discretized as

$$\begin{aligned} x(k+1)&=Gx(k)+Hu(k) \\ y(k)&=Cx(k) \end{aligned}, \tag{11}$$

where G and H are given by

$$G=e^{AT_S},\quad H=\begin{bmatrix} H_1 \mid H_2 \mid H_3 \end{bmatrix}=\int_0^{T_S} G(\tau)d\tau B.$$

In the z-domain, the converter output voltage can be written as

$$V_i(k+1)=V_i^*(k). \tag{12}$$

The corresponding plant in the continuous/discrete domain is presented in Fig. 5.

The OBD in the control system can be compensated by a state observer or sent as feedback as an extra state variable. The compensated OBD can achieve a higher control bandwidth. However, hardware uncertainty and sampling noise can ruin the accuracy of the predictor. By contrast, the case OBD feedback, which is recommended in this study, will not encounter this problem.

Therefore, by considering V_i as an extra state variable and V_i^* as a new input variable, the system can be modeled as

$$x'(k+1)=G'x'(k)+H_1'V_i^*(k)+H_2'I_l(k)+H_3'V_s(k), \tag{13}$$

where

$$x'(k)=\begin{bmatrix} x(k) & V_i(k) \end{bmatrix}^T,\quad G'=\begin{bmatrix} G & H_1 \\ 0|_{1\times 2} & 0 \end{bmatrix},$$

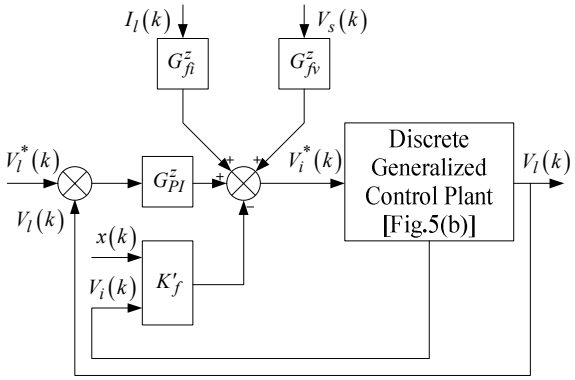


Fig. 6. Control block diagram of the proposed controller.

$$H_1'=\begin{bmatrix} 0|_{1\times 2} & 1 \end{bmatrix}^T \quad H_2'=\begin{bmatrix} H_2 & 0 \end{bmatrix}^T \quad H_3'=\begin{bmatrix} H_3 & 0 \end{bmatrix}^T.$$

B. State Feedback Control

Based on Fig. 6, the feedback vector is expressed as

$$K'_f=\begin{bmatrix} K_{V_l} & K_{I_f} & K_{V_i} \end{bmatrix}. \tag{14}$$

G_{fi}^z is the discretized load current feed-forward path and G_{fv}^z is the discretized source voltage feed-forward path, which will be discussed in the next section. The discrete proportional integral (PI) regulator is defined as

$$G_{PI}^z=K_P+\frac{K_I}{1-z^{-1}}. \tag{15}$$

The control system is of the fourth-order because of the PI regulator and OBD feedback. The system contains four poles and two zeros, and one of the zeros is invariant. Thus the residual poles and zero can be placed directly according to the desired steady-state and dynamic response. The location of the dominant complex conjugated pole pair depends on an appropriate choice of the closed-loop natural frequency and damping ratio. The non-dominant pole should be far from the dominant poles to reduce its effect. Therefore, the non-dominant pole can be placed at the origin of the z-plane. The location of the PI zero and its damping pole depends on the tuning [21]. All of the poles and PI zero are specified by

$$\begin{aligned} p_{2,3}&=e^{\left(-\zeta\pm j\sqrt{1-\zeta^2}\right)\omega_n T_s} \\ z_1&=1-0.6*\sqrt{\frac{2\pi}{\omega_n T_s}}\left[1-real(p_2)\right] \\ p_1&=0.9*z_1 \\ p_4&=0 \end{aligned}, \tag{16}$$

where ζ is the damping ratio which is set as 0.707. A higher control bandwidth results in a faster response, whereas a larger stability margin introduces less overshoot. A larger closed-loop natural frequency (ω_n) will result in a higher control bandwidth. However, it should be limited to ensure a

TABLE I

SYSTEM SPECIFICATIONS.

V_s (rated)	230 V(rms)/50 Hz
R_{load}	30 Ω
r_t	0.37 Ω
L_t	2.4 mH
C_f	50 μF
T_s	100 μs
T_{sw}	200 μs

suitable stability margin. In this study, ω_n is equal to the LC resonant frequency. For this system, the control bandwidth is 467 Hz; the gain margin is 13.4 dB; and the phase margin is 62.1°.

Further extended matrixes incorporating PI regulators are given as

$$\bar{G}=\begin{bmatrix} G' & H' \\ 0 & 0 \end{bmatrix},\quad \bar{H}=\begin{bmatrix} 0|_{3\times 1} \\ 1 \end{bmatrix}. \tag{17}$$

The desired pole vector is given as $P=\begin{bmatrix} p_1 & p_2 & p_3 & p_4 \end{bmatrix}$. The new feedback vector $\bar{K}$ can be obtained by the Ackermann function embedded in MATLAB, which is given as $\bar{K}=ac\ker\left(\bar{G},\bar{H},P\right)$. Thus the control variables can be simply obtained by

$$\begin{bmatrix} K'_f & K_I \end{bmatrix}=\left(\bar{K}+\begin{bmatrix} 0|_{1\times 3} & 1 \end{bmatrix}\right)\cdot \begin{bmatrix} G'-I_3 & H'_1 \\ (1+\alpha)C'G'-C'\alpha & (1+\alpha)C'H'_1 \end{bmatrix}^{-1} \tag{18}$$

and $K_P=\alpha K_I$, where $\alpha=z_1/(1-z_1)$ and $C'=\begin{bmatrix} C & 0 \end{bmatrix}$.

According to the parameters in Table I, the control variables can be calculated as

$$\begin{bmatrix} K'_f & K_P & K_I \end{bmatrix}=[1.2166 \quad 23.4986 \quad 0.9062 \quad 0.4986 \quad 0.3918]. \tag{19}$$

C. Feed-forward Decoupling

Accurate calculation of the feed-forward path is a key issue with regard to feed-forward decoupling. Directly acquiring a discretized feed-forward path based on a discrete state feedback controller is a complicated process. By contrast, a continuous feed-forward path can be conveniently obtained in the continuous domain [22]. Thus a discretized feed-forward path can be subsequently obtained by discretizing the continuous path.

Based on Fig. 6, the inverter voltage command in the discrete domain can be described as

$$V_i^*(k)=G_{PI}^z\left[V_l^*(k)-V_l(k)\right]-K'_f x'(k)+G_{fi}^z I_l(k)+G_{fv}^z V_s(k). \tag{20}$$

Thus Equation (20) in the continuous domain can be given as

$$V_i^*=G_{PI}^s\left(V_l^*-V_l\right)-K'_f x'+G_{fi}^s I_l+G_{fv}^s V_s, \tag{21}$$

where $G_{PI}^s=K_P+K_i/s$; $K_i=K_I/T_s$; G_{fv}^s and G_{fi}^s are the continuous feed-forward paths of the load current and source voltage; and the continuous indicator (s) has been omitted for simplicity. When $K_f=\begin{bmatrix} K_{V_l} & K_{I_f} \end{bmatrix}$, substituting Equation (21) into Equation (2) results in

$$V_i=\frac{G_{PI}^s\left(V_l^*-V_l\right)-K_f x+G_{fi}^s I_l+G_{fv}^s V_s}{e^{sT_d}+K_{V_i}}. \tag{22}$$

The continuous transfer function of the entire control system can be obtained by substituting Equation (22) into Equation (10), which is defined as Equation (23).

The continuous full feed-forward paths of the load current and source voltage can be acquired by equating the two terms, including I_l and V_s, to zero, which can be expressed as

$$\begin{aligned} G_{fi}^s&=\left(e^{sT_d}+K_{V_i}\right)\left(L_t s+r_t\right)+K_{I_f} \\ G_{fv}^s&=-e^{sT_d}-K_{V_i} \end{aligned}. \tag{24}$$

The time delay element e^{sT_d} is not numerically convergent. However, through first-order Taylor expanding, it can be linearized as

$$e^{sT_d}\approx 1+sT_d. \tag{25}$$

Thus substituting Equation (25) into Equation (24) results in,

$$\begin{aligned} G_{fi}^s&=L_t T_d s^2+\left(L_t+L_t K_{V_i}+r_t T_d\right)s+\left(1+K_{V_i}\right)r_t+K_{I_f} \\ G_{fv}^s&=-\left(1+sT_d\right)-K_{V_i} \end{aligned}. \tag{26}$$

The second-order differentiation element existing in G_{fi}^s is difficult for digital implementation. Fortunately, this element can be omitted if $L_t T_d\approx 0$. The pure differentiator is susceptible to noise. Thus a first-order pseudo differentiator with the expression $s/(1+s/\omega)$ is employed to prevent noise amplification. The modified differentiator is discretized by means of a zero-order hold. In this study, ω is selected as

$$\begin{aligned} V_l&=C*\frac{B_1 G_{PI}^s V_l^*+\left[B_3\left(e^{sT_d}+K_{V_i}\right)+B_1 G_{fi}^s\right]I_l+\left[B_2\left(e^{sT_d}+K_{V_i}\right)+B_1 G_{fv}^s\right]V_s}{\left(e^{sT_d}+K_{V_i}\right)(sI-A)+B_1 G_{PI}C+B_1 K'_f} \\ &=\frac{(K_P s+K_i)V_l^*+\left[G_{fi}^s-K_{I_f}-\left(e^{sT_d}+K_{V_i}\right)\left(L_t s+r_t\right)\right]sI_l+\left[G_{fv}^s+e^{sT_d}+K_{V_i}\right]sV_s}{\left(e^{sT_d}+K_{V_i}\right)L_t C_f s^3+\left[\left(e^{sT_d}+K_{V_i}\right)r_t C_f+K_{I_f}C_f\right]s^2+\left(e^{sT_d}+K_{V_i}+K_p+K_{V_l}\right)s+K_i} \end{aligned}, \tag{23}$$

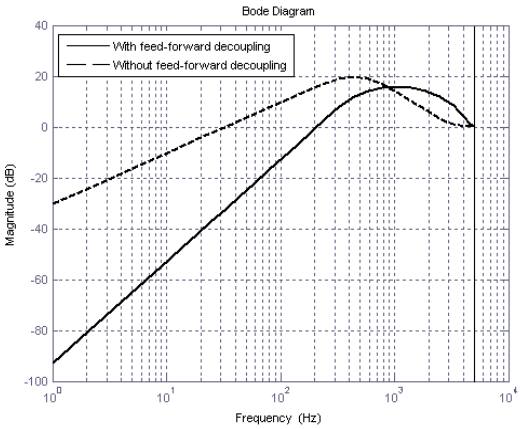


Fig. 7. Bode diagram of the closed-loop transfer function from load current to load voltage with and without load current decoupling.

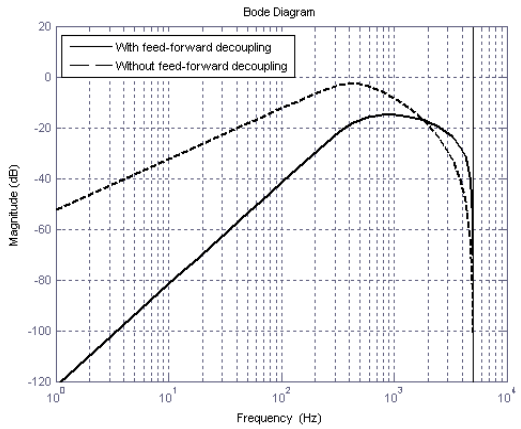


Fig. 8. Bode diagram of the closed-loop transfer function from source voltage to load voltage with and without source voltage decoupling.

1/5 of the switch frequency.

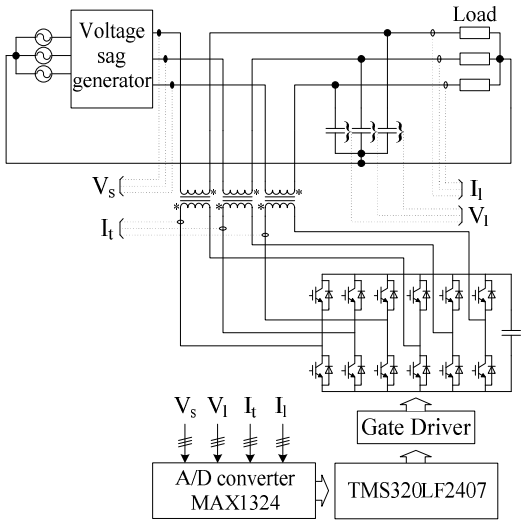
Therefore, the discretized feed-forward paths of the load current and source voltage can be defined as

$$G_{fi}^{z} = -\frac{\omega\left(L_t + L_t K_{V_i} + r_t T_d\right)\left(1 - z^{-1}\right)}{1 - e^{-\omega T_s} z^{-1}} + \left(1 + K_{V_i}\right) r_t + K_{I_f}$$
$$G_{fv}^{z} = \frac{\omega T_d \left(1 - z^{-1}\right)}{1 - e^{-\omega T_s} z^{-1}} - 1 - K_{V_i} \quad (27)$$

Fig. 7 shows a bode diagram of the closed-loop transfer function in the discrete domain from the load current to the load voltage. Fig. 8 shows a bode diagram of the closed-loop transfer function in the discrete domain from the source voltage to the load voltage.

Figs. 7 to 8 show that feed-forward decoupling possibly improves the load current/source voltage rejection capability, mainly in the low- to medium-frequency ranges. By contrast, feed-forward decoupling attenuates the capability in the high-frequency range. The reason for this outcome is that a first-order Taylor expansion is employed to linearize the time

(a)



(b)

Fig. 9. (a) Laboratory prototype of the DVR system. (b) Schematic diagram of the DVR prototype.

delay element e^{sT_d}, which will lower the accuracy of feed-forward paths. Although the feed-forward paths exhibit several deviations from ideal paths, they are still attractive choices considering their strong load current/source voltage rejection capability in low- to medium-frequency ranges and their uncomplicated implementation process.

IV. Experimental Results

A 5 kVA laboratory prototype, shown in Fig. 9, was built to verify the proposed discrete state-space controller scheme. A digital signal processor TMS320LF2407 and two extended 14-bit analog-to-digital converters (MAXIM-1324ECM) are

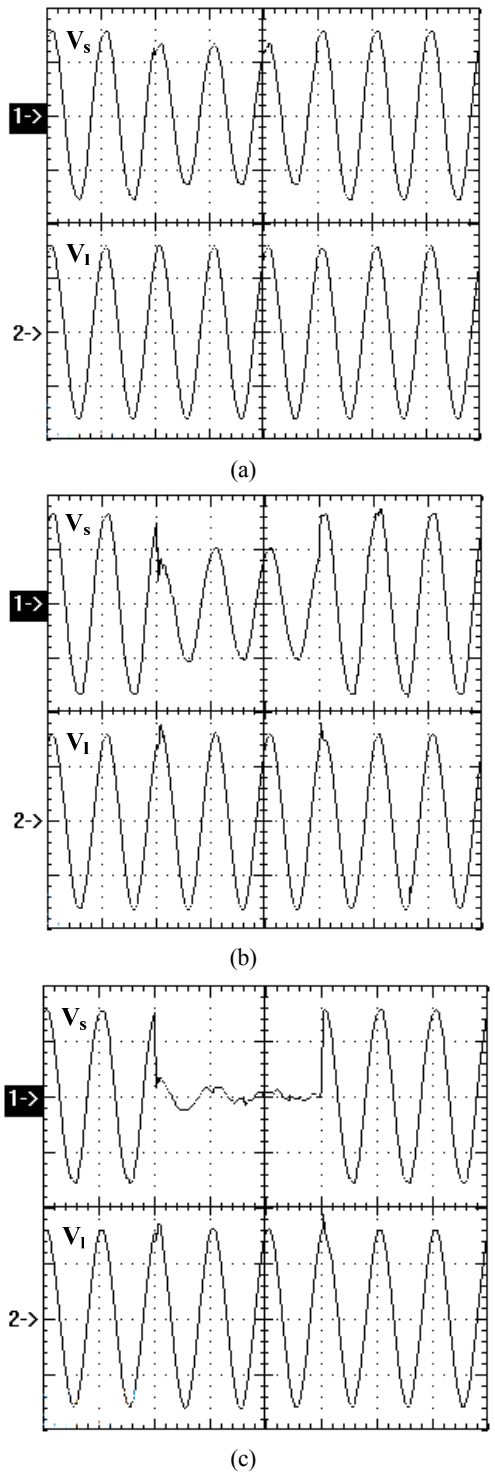


Fig. 10. Transient response to voltage sags under different sag depths: (a) Voltage sag depth: 10%, (b) voltage sag depth: 40%, and (c) voltage sag depth: 90%. (CH1: source voltage, 200 V/div; CH2: load voltage, 200 V/div; t: 20 ms/div).

used. Three isolated 1:1 transformers are connected between the line side and the converter side. The switching frequency is set to 5 kHz and the PWM sampling frequency is set to 10 kHz. Table I lists the system specifications. Symmetrical

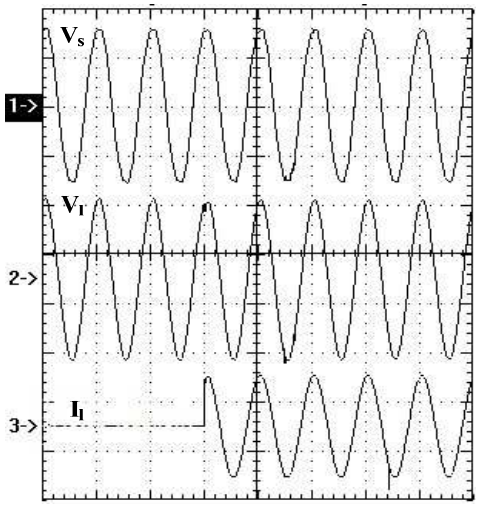


Fig. 11. Transient response to rated load added. (CH1: source voltage, 200 V/div; CH2: load voltage, 200 V/div; CH3: load current, 10 A/div; t: 20 ms/div).

voltage sags for a time interval of 60 ms are generated by a voltage-sag generator, which is combined with a three-phase autotransformer and insulated gate bipolar transistors [23].

The transient response of the DVR under the proposed discrete state-space controller has been investigated. The results corresponding to the voltage sags are shown in Fig. 10. Three voltage sag depths have been created, namely, 10%, 40%, and 90%, to strictly test the DVR in transient operation. The source voltage drops to different residual values from 40 ms to 100 ms. Considering that the load voltage control is independent in each phase, only the a-phase voltage waveform is shown for convenience. The experimental results show that the amplitude of the load voltage is kept unchanged, with a small oscillatory transient immediately following step changes in the source voltage.

To analyze the influence of load disturbances on the load voltage in transient operation, the load current is changed from zero to a rated value. Fig. 11 shows the transient response corresponding to the step change of the load current with the proposed control scheme. The load voltage remains stable, with a small transient notch, when a rated load is plugged in.

Fig. 12 depicts the steady-state harmonic compensation capability of the DVR under a linear load. The 3rd, 5th, 7th, and 9th harmonics with contents of 7.81%, 4.72%, 2.40%, and 1.79%, respectively, are introduced into the source voltage. The total harmonic distortion (THD) of the source voltage is 9.911%, whereas the THD of the load voltage is 1.759%. The result shows that the proposed control scheme is effective in suppressing distortions of the source voltage.

V. CONCLUSION

A discrete state-space control scheme is proposed for a DVR. The filter capacitor is placed on the load side of the

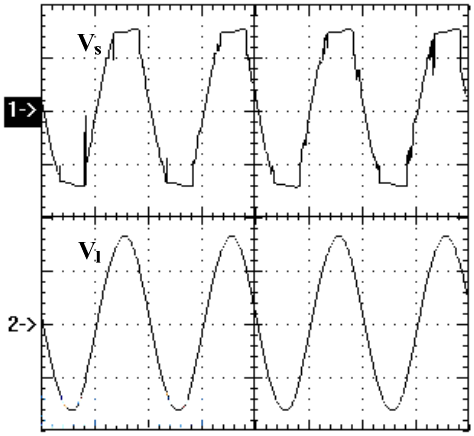


Fig. 12. Harmonic compensation in a steady-state operation. (CH1: source voltage, 200 V/div; CH2: load voltage, 200 V/div; t: 10 ms/div).

injection transformer to filter the source voltage, especially for high-frequency harmonics. Discrete state feedback control with OBD feedback improves controllability of the proposed system. Full feed-forward decoupling is adopted to stabilize the load voltage following step changes in the source voltage and load current. The main advantages of the proposed control scheme are a fast dynamic response, a strong voltage harmonic suppression, and a low computational burden. The performance of the proposed control strategy has been verified by simulation and experimental results.

REFERENCES

[1] M. H. J. Bollen, Understanding Power Quality Problems, John Willey&Sons, 2000.

[2] D. M. Vilathgamuwa, A. A. D. R. Perera, and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," *IEEE Trans. Power Del.*, Vol. 18, No. 3, pp. 928-936, Jul. 2003.

[3] C. Meyer, R. W. D. Doncker, Y. W. Li, and F. Blaabjerg, "Optimized control strategy for a medium-voltage DVR—theoretical investigations and experimental Results," *IEEE Trans. Power Electron.*, Vol. 23, No. 6, pp. 2746-2754, Nov. 2008.

[4] J. Y. Jeong, J. H. Lee, and B. M. Han, "Three-phase line-interactive dynamic voltage restorer with a new sag detection algorithm," *Journal of Power Electronics*, Vol. 10, No. 2, pp. 203-209, Mar. 2010.

[5] D. M. Vilathgamuwa, P. C. Loh, and Y. W. Li, "Protection of microgrids during utility voltage sags," *IEEE Trans. Ind. Electron.*, Vol. 53, No. 5, pp. 1427-1436, Oct. 2006.

[6] Y. W. Li, D. M. Vilathgamuwa, P. C. Loh, and F. Blaabjerg, "A dual-functional medium voltage level DVR to limit downstream fault currents," *IEEE Trans. Power Electronics*, Vol. 22, No. 4, pp. 1330-1340, Jul. 2007.

[7] F. M. Mahdianpoor, R. A. Hooshmand, and M. Ataei, "A new approach to multifunctional dynamic voltage restorer implementation for emergency control in distribution systems," *IEEE Trans. Power Delivery*, Vol. 26, No. 2, pp. 882-890, Apr. 2011.

[8] A. Ghosh, A. K. Jindal, and A. Joshi, "Design of a capacitor-supported dynamic voltage restorer (DVR) for unbalanced and distorted loads," *IEEE Trans. Power Del.*, Vol. 19, No. 1, pp. 405-413, Jan. 2004.

[9] M. J. Newman, D. G. Holmes, J. G. Nielsen, and F. Blaabjerg, "A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level," *IEEE Trans. Ind. Appl.*, Vol. 41, No. 6, pp. 1744-1753, Nov./Dec. 2005.

[10] G. F. Teng, G. C. Xiao, L. L. Hu, Y. Lu, and Y. R. Kafle, "Control strategy based on equivalent fundamental and odd Harmonic resonators for single-phase DVRs," *Journal of Power Electronics*, Vol. 12, No. 4, pp. 654-663, Jul. 2012.

[11] H. Kim and S. K. Sul, "Compensation voltage control in dynamic voltage restorers by use of feed-forward and state feedback scheme," *IEEE Trans. Power Electron.*, Vol. 20, No. 5, pp. 1169-1177, Sep. 2005.

[12] P. T. Cheng, J. M. Chen, and C. L. Ni, "Design of a state-feedback controller for series voltage-sag compensators," *IEEE Trans. Ind. Appl.*, Vol. 45, No. 1, pp. 260-267, Jan/Feb. 2009.

[13] Y. H. Cho and S. K. Sul, "Controller design for dynamic voltage restorer with harmonics compensation function," *in Proc. IAS,* pp. 1452-1457, 2004.

[14] P. R. Sánchez and E. Acha, "Dynamic voltage restorer based on flying capacitor multilevel converters operated by repetitive control," *IEEE Trans. Power Del.*, Vol. 24, No. 2, pp. 951-960, Apr. 2009.

[15] Y. W. Li, D. M. Vilathgamuwa, F. Blaabjerg, and P. C. Loh, "A robust control scheme for medium-voltage-level DVR implementation," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 4, pp. 2249-2261, Aug. 2007.

[16] Y. W. Li, F. Blaabjerg, D. M. Vilathgamuwa, and P. C. Loh, "Design and comparison of high performance stationary-frame controllers for DVR implementation," *IEEE Trans. Power Electron.*, Vol. 22, No. 2, pp. 602-612, Mar. 2007.

[17] J. D. Barros and J. F. Silva, "Multilevel optimal predictive dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2747-2760, Aug. 2010.

[18] Y. W. Li, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, "Investigation and improvement of transient response of DVR at medium voltage level," *IEEE Trans. Ind. Appl.*, Vol. 43, No. 5, pp. 1309-1319, Sep./Oct. 2007.

[19] Y. W. Li, "Control and resonance damping of voltage-source and current-source converters with LC filters," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 5, pp. 1511-1521, May. 2009.

[20] R. Turner, S. Walton, and R. Duke, "Robust high-performance inverter control using discrete direct design pole placement," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 1, pp. 348-357, Jan. 2011.

[21] M. Y. Xue, Y. Zhang, F. R. Liu, Y. Kong, and Y. X. Yi, "Optimized pole and zero placement with state observer for LCL type grid-connected inverter," *in Proceeding of ECCE*, pp. 377-382, 2011.

[22] M. Y. Xue, Y. Zhang, Y. Kong, Y. X. Yi, S. M. Li, and F. R. Liu, "Full grid voltage feed-forward for discrete state feedback controlled grid-connected inverter with LCL filter," *IEEE Trans. Power Electron.*, Vol. 27, No. 10, pp. 4234-4247, Oct. 2012.

[23] T. Jimichi, H. Fujita, and H. Akagi, "An approach to eliminating DC magnetic flux from the series transformer of a dynamic voltage restorer," *IEEE Trans. Ind. Appl.*, Vol. 44, No. 3, pp. 809-816, May/Jun. 2008.

He Lei was born in Hubei province, China, in 1985. He received his B.S. in Electrical Engineering and Automation from the Huazhong University of Science and Technology, Wuhan, China, in 2006. He is currently working toward his Ph.D. in Power Electronics and Drives from the Huazhong University of Science and Technology. His current research interests include power electronic converters and their digital control techniques.

Xin-Chun Lin was born in Hubei Province, China, in 1974. He received his Ph.D. in Electrical Engineering from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2003. He is currently an Associate Professor in the Department of Applied Power Electronic Engineering, HUST. His current research interests include dynamic voltage restorers, control techniques for power electronic apparatus and wind power generation systems.

Ming-Yu Xue was born in Zhejiang Province, China, in 1984. He received his B.S. in Electrical Engineering and Automation from the Dalian University of Technology, Dalian, China, in 2006. He received his M.S. and Ph.D. in Power Electronics and Drives from the Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2012, respectively. His current research interests include power electronic converters, renewable energy, and distributed generation.

Yong Kang was born in Hubei Province, China, on October 16, 1965. He received his B.E. M.E, and Ph.D. from the Huazhong University of Science and Technology, Wuhan China, in 1988, 1991 and 1994, respectively. In 1994, he joined the Huazhong University of Science and Technology as a Lecturer and was promoted to Associate Professor in 1996 and to Full Professor in 1998. He is presently the Head of the College of Electrical and Electronic Engineering, Huazhong University of Science and Technology. He is the author of more than 60 technical papers. His current research interests include power electronic converters, ac drivers, electromagnetic compatibility, and their digital control techniques.