A New DC/DC Converter With Wide-Range ZVS and Reduced Circulating Current

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***Abstract*—A new three-level dc/dc converter is proposed in this paper. The outstanding features of this converter are that it operates with zero-voltage-switching (ZVS) from full-load to near no-load conditions with hardly any circulating freewheeling primary current due to its novel structure. Since the converter has little primary circulating current and its switches are exposed to only half of the input voltage, it has high efficiency even under light loads. In this paper, the new converter is introduced, its basic operating principles are explained, its modes of operation and its steady-state characteristics are discussed in detail as is its design, and experimental results obtained from a prototype converter that confirm its feasibility are presented.**

***Index Terms*—DC/DC power conversion, phase-shifted modulation (PSM) converters, switch-mode power supply, zero-voltage-switching (ZVS).**

I. Introduction

ONE of the most popular topologies for high-power (>500 W) and high-density converter designs is the two-level, zero-voltage-switching (ZVS) pulse width modulation (PWM), full-bridge (FB) dc/dc converter as shown in Fig. 1 [1]. The converter operates with inherent ZVS turn-on of its switches as available primary transformer energy is used to discharge the output capacitances of the switches just before they are turned ON. This is especially true when the converter is operating under heavy load conditions and as it can be seen in Fig. 2 in light load conditions the converter loses its ZVS turn-on due to lack of enough energy to discharge the body capacitance of the switches.

When the ZVS-PWM-FB converter enters a freewheeling mode of operation (see Fig. 3), however, no voltage is impressed across its transformer primary. What this means is that no energy is transferred from the transformer primary to its secondary and current just circulates in the converter and creates conduction losses. Circulating current and ZVS capability are inversely related as more circulating current means a wider load range for ZVS operation as there is more energy available to discharge the switch output capacitances. This results in fewer switching losses, but more conduction losses.

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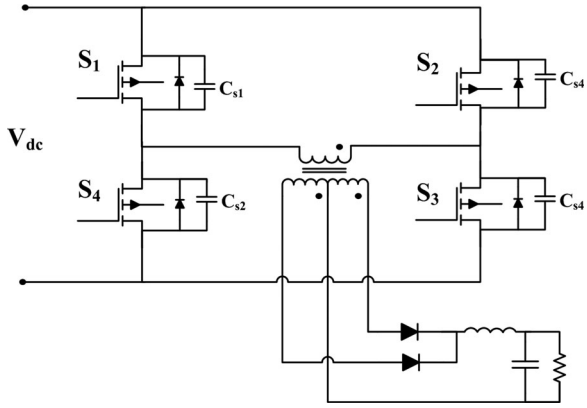

Fig. 1. ZVS FB dc–dc converter.

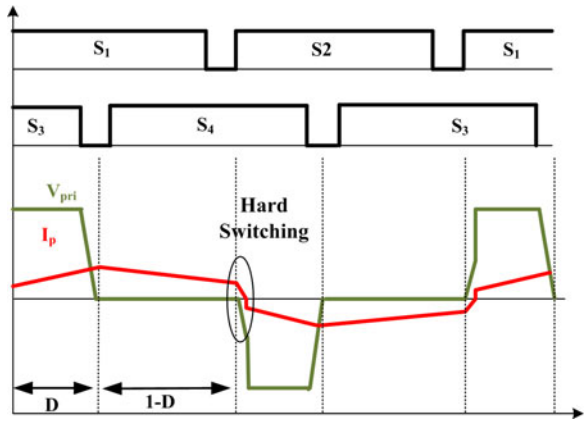

Fig. 2. Losing ZVS for ZVS-FB dc–dc converter at light load conditions.

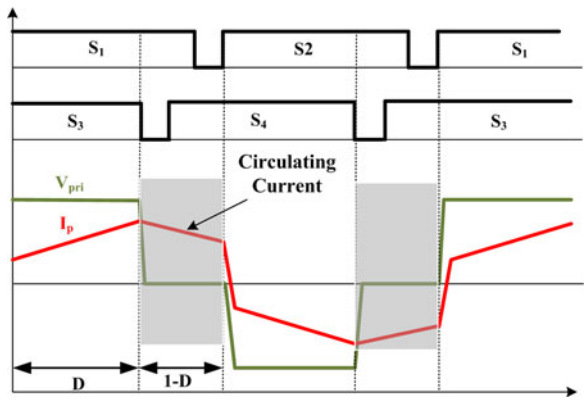

Fig. 3. Freewheeling mode of operation for ZVS-FB dc–dc converter.

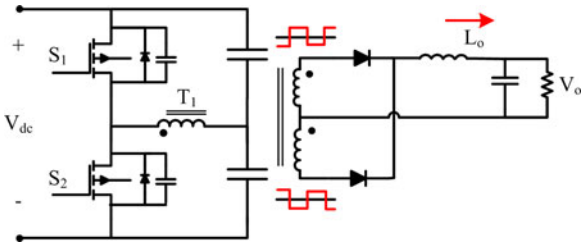

Fig. 4. HB converter.

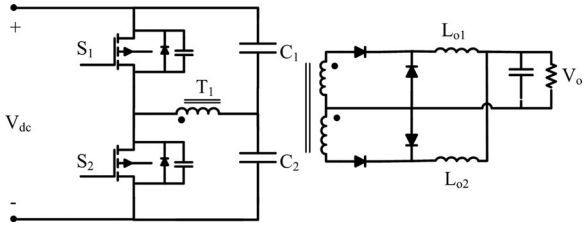

Fig. 5. Modified HB converter.

It is, therefore, standard practice for ZVS-PWM-FB converter designs that the range of ZVS operation be limited to loads greater than 25%–50% full load so that conduction losses caused by circulating current do not become excessive. But regardless of whatever compromise is made between circulating current and ZVS range, there are two main weaknesses for the ZVS-PWM-FB topology for high-voltage applications; one of them is its poor light load efficiency and another one is the voltage stress across the switches.

Attempts have been made to increase the efficiency of FB dc/dc converters by addressing this issue of circulating current versus ZVS range, but most of these attempts have been flawed in some way. For example, converters that use zero-voltage–zero-current methods to eliminate the freewheeling mode circulating current [2]–[8] or use passive auxiliary circuits to extend the ZVS range [9]–[15] offer modest improvement over the ZVS-PWM-FB converter for light loads.

Three-level dc/dc converters have been presented in [16]–[22] to reduce the voltage stress across the switches. The voltage stresses of their power switches are only half of the input voltage and not the full input voltage as is the case for two-level converters. This means that less energy is required to discharge the output capacitances of switch MOSFET devices and thus they can operate with fewer switching losses and a wider load range for ZVS than two-level converters. The circulating current in three-level converters, however, can be twice as much as that found in comparable two-level converters so that they have more conduction losses. These conduction losses can offset the gain in efficiency that is made with the extension of the load range for ZVS.

This paper proposes a new dc/dc converter that tries to take advantage of the lower switch voltage stress of three-level converters, but with minimal circulating current so that excellent converter efficiency can be achieved. In this paper, the new converter is introduced, its basic operating principles are explained, and its modes of operation and characteristics are discussed. The feasibility of the proposed converter is confirmed with experimental results obtained from a prototype converter.

II. Basic Principles

The main principle of the proposed converter is based on half-bridge (HB) dc–dc converters as shown in Fig. 4. Operating the converter with the gating signals of the switches set at 50% of the duty cycle is the most attractive way to operate an HB converter. This is because the converter has no circulating current when operating with such gating signals and each capacitor has approximately the same voltage across it. Moreover, the HB converter works with soft switching over a wide load range without using snubber circuits.

The HB converter can be modified to have the topology shown in Fig. 5. This converter consists of an HB inverter and a full-wave rectification circuit and a current-doubler output. This converter has the same advantages of the HB converter while the converter's secondary acts as two interleaved forward converter outputs connected in parallel and 180° phase offset between the two outputs. The power transformer and the output inductors operate in such a way that switches can maintain ZVS over a wide load range.

Although it is advantageous to operate an HB converter with its switches operating with 50% duty cycle, fixing the duty cycle means that the converter cannot regulate its output voltage. Several converters that combine two HB converters in their topologies and regulate the output voltage by some other means have been proposed in the literature to take advantage of the benefits of operating an HB converter with 50% duty cycle [23]–[26]. The topology proposed in [23] and [24] uses two HB converters series at the input and series at the output with an interleaved phase-shift strategy. This converter has some advantages such as a wide load range ZVS for its switches and a voltage stress for each switch that is half of the dc bus voltage; however, this converter has the same issues that ZVS-PWM-FB converters have related to circulating current when it is in a freewheeling mode so that it suffers from conduction losses under heavy load conditions.

The converter proposed in [25] is a two-stage converter that combines a buck converter stage with an HB converter. The first stage is the buck converter stage, which is used to regulate the input of the HB converter, which is made to operate with a 50% duty cycle. The buck converter stage can regulate the output and the voltage stress of the converter switches is half of the dc bus voltage; however, the switches of buck converters turn ON without ZVS, which affects converter efficiency.

Another topology proposed in [26] is combines two of the modified HB converters shown in Fig. 5 by connecting them in parallel at the input and output. This converter can operate with ZVS over a wide load range and does not have any circulating current due to freewheeling modes of operation. The voltage stress of each switch, however, is equal to the dc bus voltage so that the same amount of energy is required to discharge the output switch capacitances as for the output capacitances in two-level converters, which means that the light load efficiency is still not good.

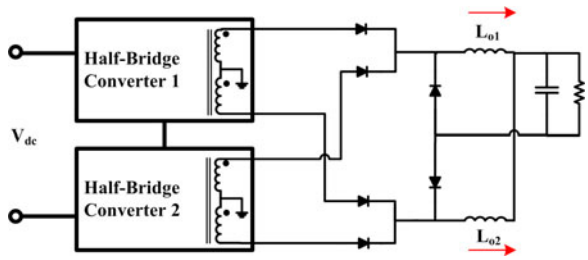

Fig. 6. Block diagram of the proposed converter.

A new dc/dc converter is proposed in this paper. The proposed converter has HB converters connected to the input together in series as shown in Fig. 6, with: 1) one converter stacked on top of the other; 2) a PWM technique that phase shifts the transformer voltage of one of the HBs with respect to the other; and 3) the secondary outputs of the two converters superimposed on a common output filter. The overall dc/dc converter can operate with the ZVS advantages and zero circulating current of an HB converter, but with output voltage regulation. Moreover, the proposed converter arrangement reduces the voltage ratings of the switches so that it can operate with improved light load efficiency.

III. Converter Operation

The proposed dc/dc converter, shown in Fig. 7, is made up of two HB converters stacked one on top of the other. Each HB has an inductor ($L_r = L_{r1} = L_{r2}$) and two clamping diodes that are added to the basic HB topology. The inductor stores extra energy to extend the ZVS range while the clamping diodes minimize any voltage ringing that may appear on either side of the transformer.

As stated in the previous section, each HB is operated with a 50% duty cycle and can be phase shifted from 0° to 180° with respect to the other. This phase shifting affects the voltage that is delivered to the current doubler filter input nodes F_1 and F_2, V_{F1} and V_{F2}. When the phase-shift is 0°, Fig. 8, there is no overlap between V_{F1} and V_{F2}, the converter's duty cycle is 50%, and the net output voltage, V_o, is at its minimum. When the phase-shift is 180°, Fig. 9, there is complete overlap between V_{F1} and V_{F2}, the converter's duty cycle is 100%, and V_o is at its maximum. The output voltage can be regulated by phase-shifting the two HBs from full load to very light load conditions (see Figs. 10 and 11). Key waveforms with the phase-shift control are shown in Fig. 12. If the power transformer's turn ratio is N:1:1, the converter input and output voltage relationship is described as

$$V_o = \frac{V_{\rm dc}}{4} * \left(\frac{0.5 + (\varphi/360)}{N}\right) \tag{1}$$

and the converter's duty cycle is

$$D = 0.5 + \frac{\varphi}{360}. \tag{2}$$

It should be noted that this converter actually transfers power from the primary to the secondary during both D and 1 – D periods. It is because of the fact that the converter has two HB converters in such a way that they always transfer energy from input to the output.

The converter has the following modes of operation. It is assumed that $L_{o1} = L_{o2}$, $C_1 = C_2 = C_3 = C_4$, turns ratio of T_1 = turns ratio of $T_2 = N$ and lower HB has a phase-shift φ respect to the upper HB. The key waveforms and the equivalent circuit for each mode of operation are shown in Figs. 12 and 13, respectively.

A. Mode 1 ($t_1 \le t \le t_2$) (Separate Power Transferring for Each HB)

During this mode, switches S_1 and S_4 are ON. The voltage across the primary of T_1 is positive and the voltage across the primary of T_2 is negative and diodes D_5 and D_8 conduct. Energy is transferred from the primary side to the secondary side of both T_1 and T_2. In this mode, each HB separately transfers energy to the output. The voltage across the output inductors L_{o1} and L_{o2} are the same and equal to $(V_{\rm dc}/4N) - V_o$ and inductor currents i_{Lo1} and i_{Lo2} are increasing. The duration of this mode depends on the phase-shift degree φ.

B. Mode 2 ($t_2 \le t \le t_3$) (Lower HB Transition)

At t_2, S_4 is turned OFF and capacitor C_{S4} is charged and C_{S3} is discharged in resonant fashion. The primary current of T_2 also starts resonating down to zero. To be able to achieve ZVS during this transition, the resonant peak of the capacitor C_{S4} has to be higher than $V_{\rm dc}/2$. The equations describe this mode are

$$i_{Lr2} = (C_{\rm S3} + C_{\rm S4})\frac{dV_{\rm S4}}{dt}$$
$$L_{r2}\frac{d_{i_{Lr2}}}{dt} + V_{\rm S4} = 0 \tag{3}$$

therefore

$$i_{Lr2}(t) = I_p \cos(\omega_r t)$$
$$v_{\rm S4}(t) = Z_r I_p \cos(\omega_r t) \tag{4}$$

where

$$\omega_r = \frac{1}{\sqrt{(L_{r2} \times (C_{\rm S3} + C_{\rm S4}))}}$$
$$Z_r = \sqrt{\frac{L_{r2}}{C_{\rm S3} + C_{\rm S4}}}. \tag{5}$$

In order to achieve ZVS for S_3, it needs to have a delay time t_d before S_3 turns ON, for the primary current of T_2 to discharge completely the body capacitor of S_3 and conduct the body diode of S_3. According to (4) and (5) t_d can be expressed by

$$t_d = \sin^{-1}\left(\frac{V_{\rm dc}/(2 \times I_p \times Z_r)}{\omega_r}\right)$$
$$t_d \le \frac{\pi}{2\omega_r}. \tag{6}$$

During this mode, the primary voltage across T_2 reverses its polarity and becomes positive, which causes diode D_{10} to conduct and take over current i_{Lo2} from D_8. The top HB maintains its

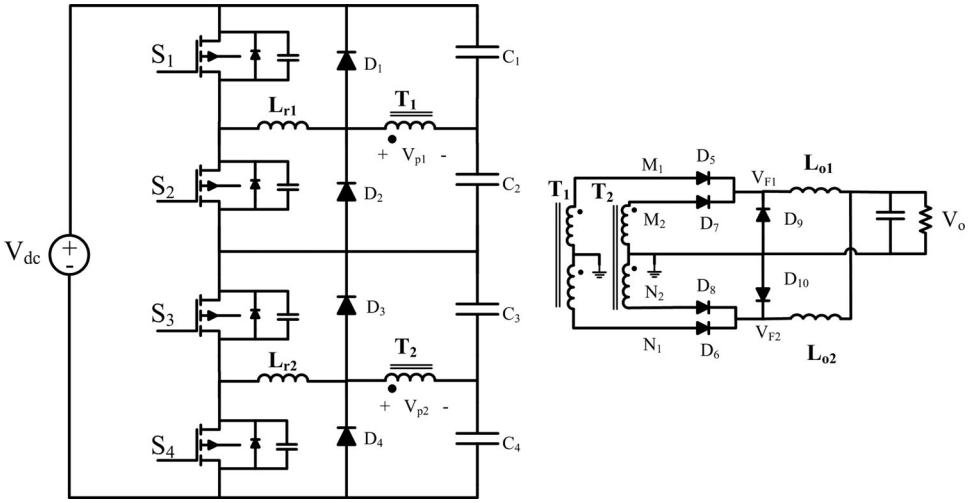

Fig. 7. Proposed dc–dc converter.

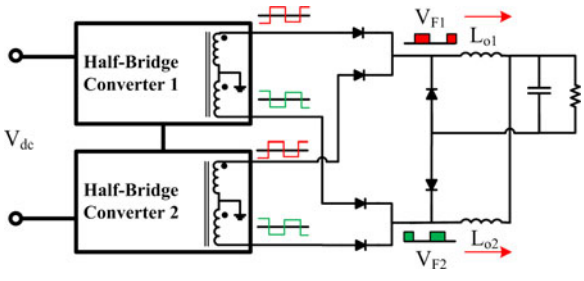

Fig. 8. Proposed converter with zero-degree phase shift.

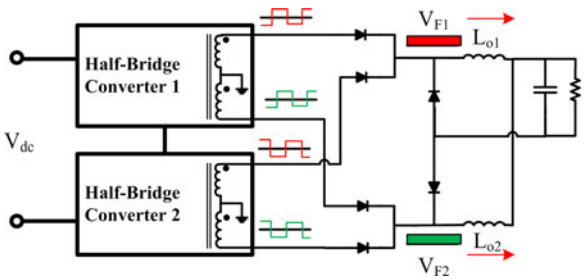

Fig. 9. Proposed converter with 180° phase shift.

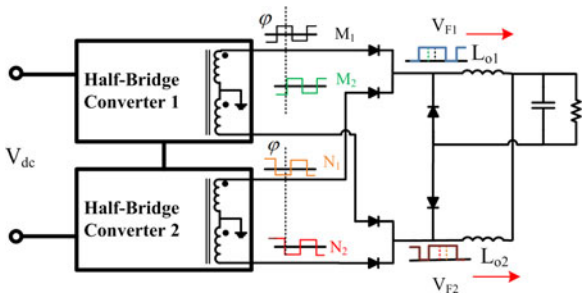

Fig. 10. Proposed converter with φ degree phase shift.

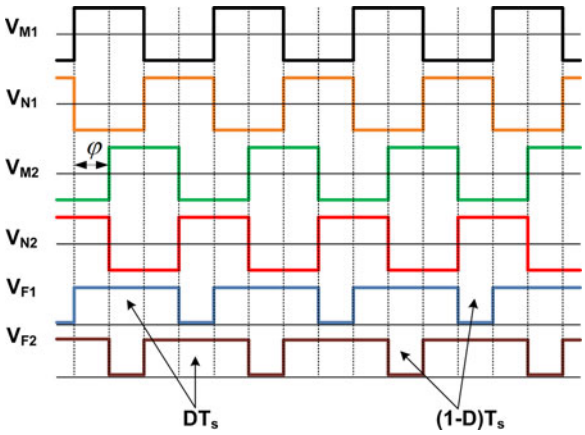

Fig. 11. Waveforms with phase-shift control.

previous state and continues to apply a voltage to F_1 through diode D_5.

C. Mode 3 ($t_3 \leq t \leq t_4$) (Power Sharing)

This mode starts when S_3 turns ON with ZVS. The polarity of T_1 and T_2 are both positive and diodes D_5 and D_7 both conduct and share output current, i_{Lo1} since the two transformer outputs, V_{M1} and V_{M2}, have almost the same voltage. In the meantime, D_{10} continues to conduct current i_{Lo2} and i_{Lo2} starts to decrease as $-V_o$ is applied to L_{o2}. The decrease of i_{Lo2} and the increase of i_{Lo1} lead to current ripple cancellation and output current ripple minimization.

D. Mode 4 ($t_4 \leq t \leq t_5$) (Upper HB Transition)

At t_4, S_1 is turned OFF and C_{S2} is discharged and C_{S1} is charged in resonant fashion. The primary current of T_1 also starts resonating down to zero. To be able to achieve ZVS during this transition, the resonant peak of the capacitor C_{S1} has to be higher than $V_{\rm dc}/2$. In this mode, the delay time should be the

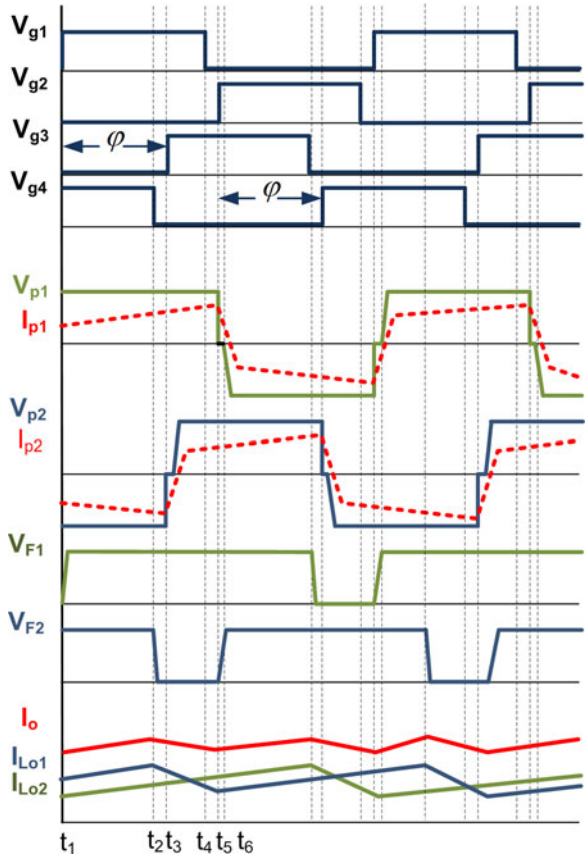

Fig. 12. Typical waveforms describing modes of operation.

same as that for Mode 2

$$t_d = \sin^{-1}\left(\frac{V_{\rm dc}/(2 \times I_p \times Z_r)}{\omega_r}\right)$$
$$t_d \le \frac{\pi}{2\omega_r} \tag{7}$$

where I_p is the maximum transformer current and

$$\omega_r = \frac{1}{\sqrt{(L_{r1} \times (C_{\rm S1} + C_{\rm S2}))}}$$
$$Z_r = \sqrt{\frac{L_{r1}}{C_{\rm S1} + C_{\rm S2}}} \tag{8}$$

to achieve ZVS for S_2. The body-diode of S_1 starts to conduct and continues. The voltage across T_1 starts to decrease and eventually reverses its polarity. Output inductor current i_{Lo2} still continues to flow through D_{10} until D_6 starts to conduct.

E. Mode 5 ($t_5 \le t \le t_6$) (Separate Power Transferring for Each HB)

After S_2 is turned ON with ZVS at t_5, inductor current i_{Lr2} decreases to zero quickly and then starts to build up in the opposite direction. When the i_{Lr2} current reflected to the secondary becomes greater than i_{Lo2} then current is transferred from D_{10} to D_6. In this mode, each HB separately transfers energy to the output. The voltage across the output inductors L_{o1} and L_{o2} are the same and equal to $(V_{\rm dc}/4N) - V_o$ and inductor currents i_{Lo1} and i_{Lo2} are increasing.

Time t_6 is the end of the half-switching cycle and another half-switching cycle begins with the same modes, but with complimentary devices conducting current. Each switching cycle has two such half-switching cycles.

The proposed converter has the following features:

1) It can operate with ZVS from full-load to near no-load conditions. This is because each converter switch is part of an HB converter that operates with 50% duty cycle. Since an HB converter with 50% duty cycle does not operate with any freewheeling modes of operation as does a FB converter, there will always be sufficient energy to discharge the output switch capacitances.
2) In addition to the fact that each converter switch is in an HB converter, it is exposed to only half the input voltage as the converter has two HB converter arranged in a multilevel structure. As a result, less energy is needed to discharge the output capacitor of each converter switch, which further extends the load range over which the converter can operate with ZVS to near no-load conditions.

Since the converter consists of two HB converters, which do not have freewheeling modes of operation, the converter has near zero circulating current as it transfers energy to the load during all modes of operation. This is another source of efficiency improvement.

IV. Design Procedure

A design procedure for the proposed converter is given along with an example to demonstrate how the converter can be designed. The converter is to be designed with the following parameters for the example:

input voltage: $V_{\rm dc} = 550$ V;
output voltage: $V_o = 48$ V;
maximum output power: $P_o = 1.2$ kW;
switching frequency: $f_{\rm sw} = 1/T_{\rm sw} = 50$ kHz.

A. Transformers Turn Ratio and Resonant Inductor

The transformer turns ratio should be chosen with potential duty-cycle reduction in mind. Duty-cycle reduction is due to the presence of inductors ($L_r = L_{r1} = L_{r2}$) that are in series with each transformer leakage inductance. As was stated at the beginning of Section III, each HB has an inductor ($L_r = L_{r1} = L_{r2}$) and two clamping diodes that are added to the basic HB topology. The inductor stores extra energy to extend the ZVS range while the clamping diodes minimize any voltage ringing that may appear on either side of the transformer.

The L_{r1} and L_{r2} resonant inductors cause a finite slope of rising and falling primary current edges that impact the secondary voltage as shown in Fig. 14 [27]. Based on Fig. 14, the duty-cycle reduction can be expressed as

$$\Delta V = L_r \frac{\Delta I}{\Delta t} \tag{9}$$

and

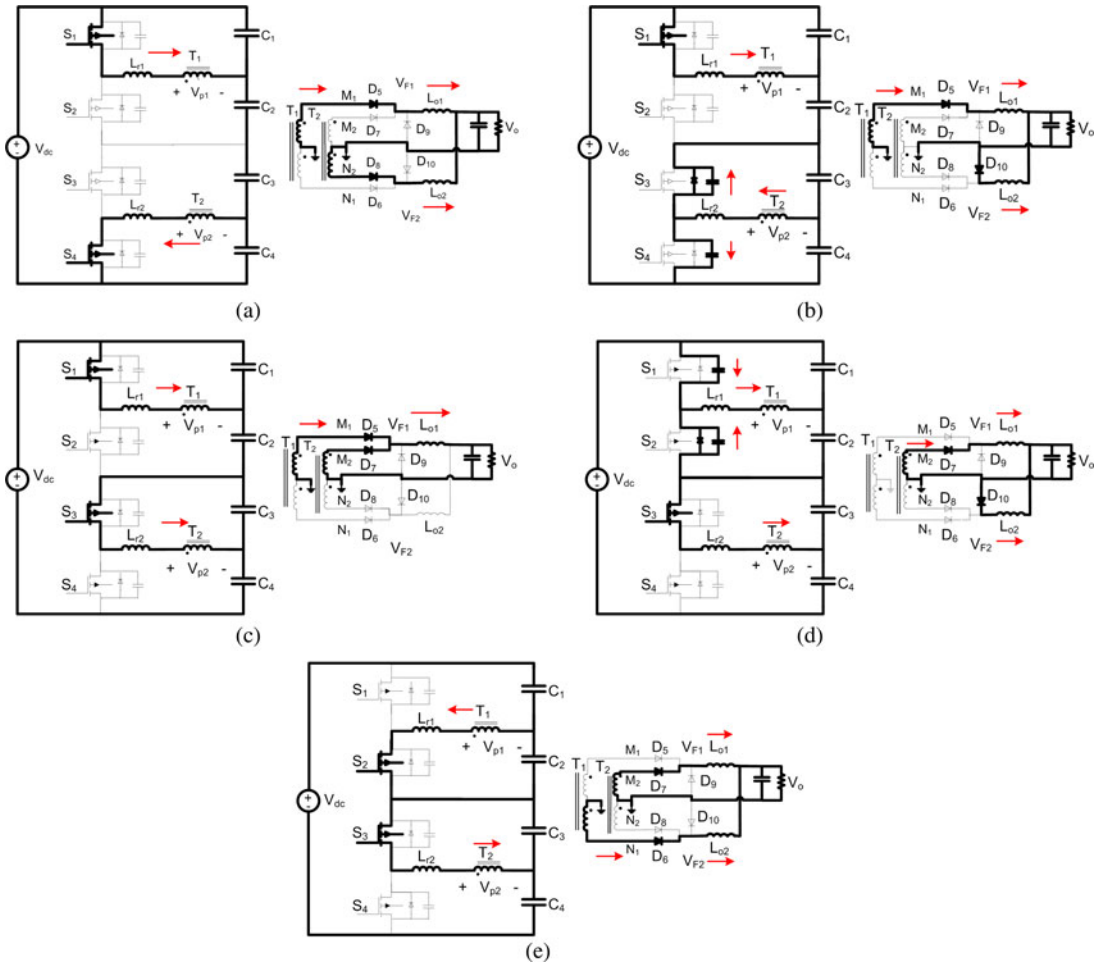

Fig. 13. Modes of operation. (a) Mode 1 ($t_1 < t < t_2$). (b) Mode 2 ($t_2 < t < t_3$). (c) Mode 3 ($t_3 < t < t_4$). (d) Mode 4 ($t_4 < t < t_5$). (e) Mode 5 ($t_5 < t < t_6$).

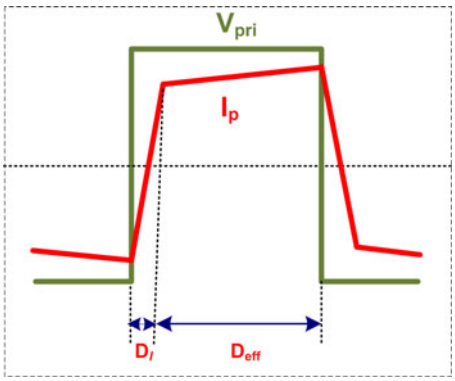

Fig. 14. Effect of series inductor on duty cycle.

$$\frac{V_{\rm dc}}{2} = L_r \frac{2I_o}{\Delta D_l (T_{\rm sw}/2)} \tag{10}$$

therefore

$$D_l = \frac{8L_r I_o}{NV_{\rm dc}T_{\rm sw}} \tag{11}$$

where $L_r = L_{r1} = L_{r2}$ is the resonant inductor and I_o is the maximum output load current, N is the transformer turns ratio, $V_{\rm dc}$ is the dc bus voltage and $T_{\rm sw}$ is the switching period. The effective duty cycle can be expressed as

$$D_{\rm eff} = D - D_l. \tag{12}$$

By substituting (2) and (11) in (12)

$$D_{\rm eff} = 0.5 + \frac{\varphi}{360} - \frac{8L_r I_o}{NV_{\rm dc}T_{\rm sw}}. \tag{13}$$

Fig. 15 shows the relation between the effective duty cycle and the resonant inductance value, for $\varphi = 180°$. Fig. 15 shows that when the value of inductor increases the effect duty cycle will decrease. By substituting (5) in (13)

$$V_o = \frac{V_{\rm dc}}{4} * \left(\frac{D_{\rm eff}}{N}\right)$$

$$V_o = \frac{V_{\rm dc}}{4N} * \left(0.5 + \frac{\varphi}{360} - \frac{8L_r I_o}{NV_{\rm dc}T_{\rm sw}}\right). \tag{14}$$

Based on (14), the transformer turns ratio N can be obtained as (15)

$$N = \frac{V_{\rm dc}D + \sqrt{(V_{\rm dc}D)^2 - 128V_o f_s L_r I_o}}{8V_o}. \tag{15}$$

Fig. 16 shows the relation between the transformers turns ratio and the resonant inductance of the transformers for $V_{\rm dc} = 550$ V,

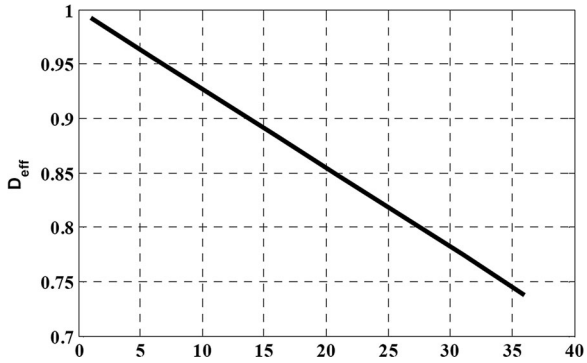

Fig. 15. Effective duty cycle versus resonant inductance.

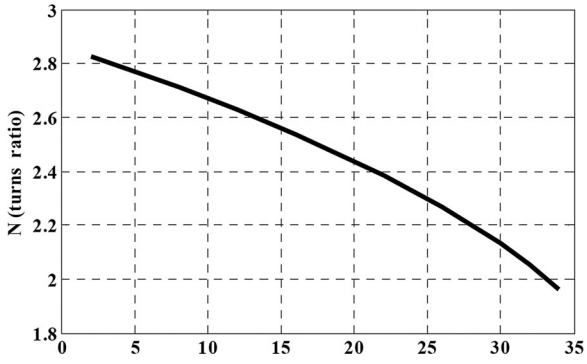

Fig. 16. Transformers turns ratio versus transformers resonant inductance.

$V_o = 48$ V, $f_s = 50$ kHz, $P_o = 1.2$ kW. As it can be seen in Fig. 16, when the value of inductor increases the transformer turns ratio should be decreased. Based on Figs. 15 and 16, the desired value for N and L_r can be determined. For this example, $N = 2.5$ and $L_r = L_{r1} = L_{r2} = 15$ μH are chosen.

B. Delay Time for ZVS

Based on (6), to have ZVS the delay time, which is the amount of time between the turning OFF of one HB switch and the turning ON of another in the same HB is

$$t_{d1} < \frac{\pi}{2}\sqrt{L_r\,(C_{Q1} + C_{Q2})} \tag{16}$$

$$t_{d2} < \frac{\pi}{2}\sqrt{L_r\,(C_{Q3} + C_{Q4})}. \tag{17}$$

This is based on a quarter of the resonant cycle interaction between L_r and the output capacitances of the switches.

C. Input Capacitors

Assuming that the four input capacitors each have the same voltage, the high-frequency voltage ripple across the capacitors can be calculated by considering the current through the capacitors in a switching cycle. The maximum peak–peak ripple of an input capacitor can be approximated by considering that at most, half of the maximum reflected load current can charge or discharge the capacitor over 50% of the switching cycle. This can be stated as

$$\Delta V_{C\,\mathrm{in}} = \frac{I_o T_s}{4N C_{\mathrm{in}}}. \tag{18}$$

The value of each input capacitor can be obtained by rearranging (18) to give

$$C_{\mathrm{in}} = \frac{I_o T_s}{4N \Delta V_{C\,\mathrm{in}}}. \tag{19}$$

If $\Delta V_{C\,\mathrm{in}} = 0.2$ V, then the value for each capacitor should be 208 μF. For this example, the value for $C_1 = C_2 = C_3 = C_4$ is chosen to be 220 μF.

If there is any voltage difference between the two secondary windings of the two transformers in parallel, the converter works the same as it does for all the modes of operation shown in Fig. 13 except for Mode 3. There are two cases for this mode.

Case 1: V_{M1} is larger than V_{M2}. In this case, D_5 continues to conduct current as it does in previous modes. D_7 cannot conduct current until the end of this mode, when the polarity of the V_{M1} changes. This means that only the HB converter with T_1 delivers power to the output during Mode 3.

Case 2: V_{M2} is larger than V_{M1}. In this case, D_5 conducts current at the start of Mode 3, but current is transferred from D_5 to D_7 during this Mode. This means that only the HB converter with T_2 delivers power to the output during Mode 3.

As a result, one converter delivers more power to the output than the other if there is any voltage difference between the two secondary windings of the two transformers. The amount of power difference depends on the amount of phase shifting between the two HB converters. For example, the phase shift varies from 20° to 110° for the converter design in this paper, which can result in one HB converter delivering as much as (110−20)/360% = 25% more power to the output than the other.

V. Experimental Results

A 1.2 kW, 550 V/48 V, 50 kHz dc/dc prototype was built to confirm the feasibility of the converter. The converter was implemented with the following component values:

power MOSFETs: IRFP460;
rectifier diodes: V30200C;
freewheel diodes: V20100;
resonant inductor: 10 μH;
output inductor: 25 μH;
power transformer: turn ratio = 25:10:10;
HB capacitors: 4 × 220 μF.

Typical converter waveforms are shown in Fig. 17. Fig. 17(a) shows typical gating and drain-source voltage waveforms of a switch. It shows that even at near zero load, the converter switches work with ZVS as the drain-source voltage of a switch can be forced down to zero before the switch is turned ON. Fig. 17(b) shows the primary voltage and current of the T_1 transformer for light load (5% of the full load). It shows that the HB switches operate with 50% duty cycle and there is no circulating current in the circuit, even for light load. Fig. 17(c) shows voltage V_{M1} and V_{M2}; it can be seen that the two voltages are phase shifted relative to each other. Fig. 17(d) shows that there

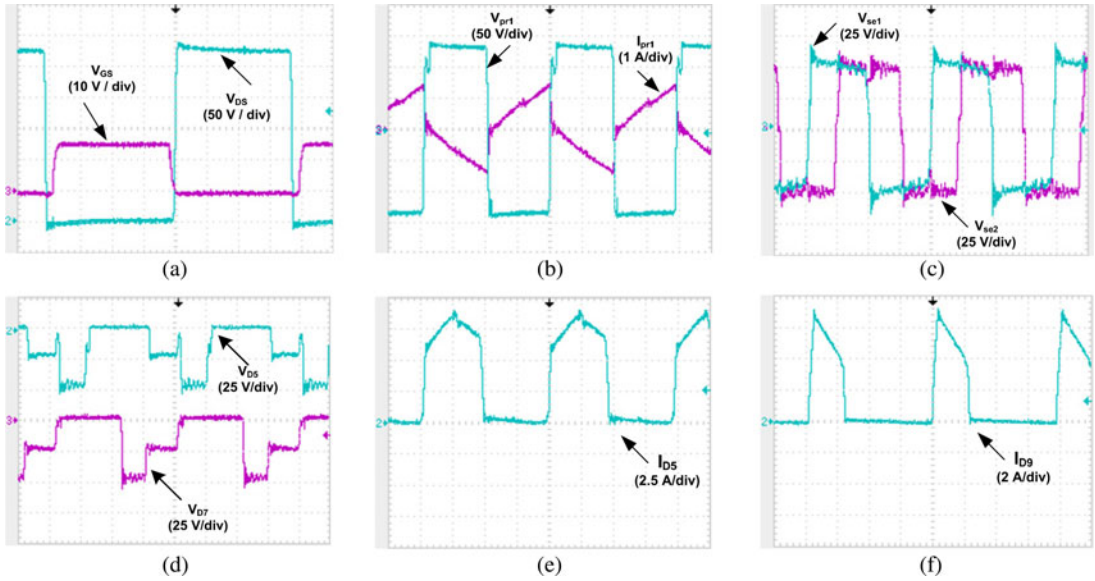

Fig. 17. Typical converter waveforms. (a) Gate and drain-source waveforms for no-load ($P_o = 60$ W). (b) Transformer primary voltage and current waveforms ($P_o = 60$ W). (c) Transformer secondary voltage waveforms ($P_o = 900$ W). (d) Voltages of rectifier diodes ($P_o = 900$ W). (e) Current of a rectifier diode ($P_o = 1200$ W). (f) Current of a freewheeling diode ($P_o = 1200$ W).

is no ringing at the output rectifiers. This is due to the presence of the clamping diodes at the primaries of both transformers.

It should be noted that no converter diode has reverse recovery issues. In the case of the primary side diodes, there is no reverse recovery because the diodes turn ON and OFF softly due to the presence of inductances in the converter. For example, two primary side diodes are connected to a common node with the cathode of one connected to the anode of another. At this node, there is a connection for the main power transformer and a resonant inductor. Any rise or fall of current in the primary diodes is, therefore, constrained by inductances and thus there is no reverse recovery current in these diodes.

As for the secondary diodes, there is no reverse recovery because the commutation of the current from a conducting diode to another diode is affected by the leakage inductances of the transformer and by the lack of sufficient voltage to force the commutation. Fig. 17(e) and (f) shows the rectifier diode current and freewheeling diode current, respectively. It can be seen that neither diode has any reverse recovery current.

Fig. 18 shows the efficiency of the proposed converter compared to other, previously proposed three-level dc/dc converters operating at 50 kHz. The most important characteristic to note is the "flatness" of the efficiency curve of the proposed converter—the proposed converter can operate with an excellent efficiency even under light load conditions while other converter have a significantly lower light load efficiency. This is because of the lack of freewheeling circulating current in the transformer primary and the fact that the converter can operate with ZVS over almost the full load range (except for the very lightest of loads). In Fig. 18, the converter can still operate with ZVS at 25 W output power (2% of full load) and experimental results show that its switches can turn ON with ZVS even at 0.5% of full load. The input voltage is 550 V and the output voltage is 48 V for the efficiency curve.

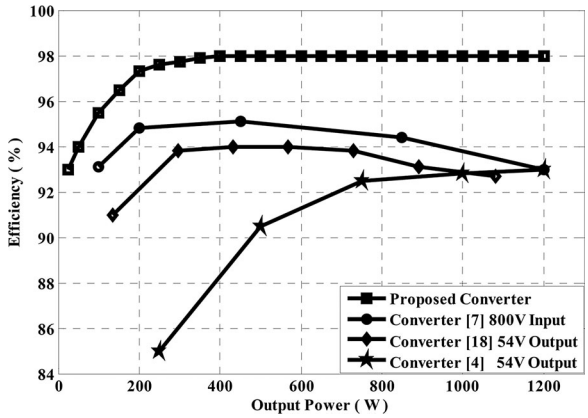

Fig. 18. Efficiency of the proposed converter at different output power.

VI. Conclusion

A new three-level dc/dc converter is proposed in this paper. The outstanding features of this converter are that it operates with ZVS from full-load to near no-load conditions with hardly any circulating freewheeling primary current due to its novel structure. This structure is based on stacking two HB converters that operate with 50% duty cycle on top of each other and voltage regulation is performed by phase-shifting one HB with respect to the other. Since such HB converters do not have freewheeling modes of operation and since the converter switches are exposed to only half the input voltage, the converter has high efficiency even under light load conditions; 95% for 10% of full load. In this paper, the basic operation of the converter was explained, its features were stated, and its design was discussed. The feasibility of the converter has been experimentally confirmed with results obtained from a prototype.

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