A Two-Phase Interleaved Power Factor Correction Boost Converter With a Variation-Tolerant Phase Shifting Technique

Yong-Seong Roh, Young-Jin Moon, Jeongpyo Park, and Changsik Yoo, *Member, IEEE*

***Abstract*—This paper presents a two-phase interleaved critical conduction mode (CRM) power factor correction boost converter with a variation-tolerant phase shifter (VTPS), which ensures accurate 180° phase shift between the two interleaved converters. A feedback loop similar to a phase-locked loop controls the amount of the phase shifting of the VTPS. The proposed VTPS has better immunity of process, supply, and temperature variations than the conventional phase shifter. A 320-W two-phase interleaved CRM boost converter prototype has been implemented, while the proposed VTPS and conventional interleaving phase shifter can be selectively applied to compare the performance of the proposed technique with the conventional one. Experimental results show that the two-phase interleaved CRM boost converter has better performance with the proposed VTPS. The proposed VTPS circuit can be applied to any type of interleaved switching power converter.**

***Index Terms*—Critical conduction mode (CRM), interleaved boost converter, power factor correction (PFC), variation-tolerant phase shifter (VTPS).**

I. Introduction

POWER factor (PF) defined as the ratio of real power to apparent power is desired to be 100% because the smaller the PF, the larger the power loss and harmonics, which may travel down the power line and disrupt other devices connected to the line [1], [2]. For a higher PF, a power factor correction (PFC) circuit is employed which shapes the input current waveform to be in phase with the input voltage waveform [3]. PFC circuits can be classified as either passive or active PFC among which active PFC is preferred due to its small form factor and higher PF [4]. The operation modes of an active PFC converter can be classified as the continuous conduction mode (CCM), discontinuous conduction mode (DCM), or critical conduction mode (CRM) depending on the current flowing through the inductor [3]. For a heavy load, the CCM is usually employed because it can handle more current than the DCM and CRM [5]. At the CCM, however, the hard switching of the freewheeling diode may result in decreased power conversion efficiency. On the contrary, the freewheeling diode is switched softly at the DCM and CRM and thus higher power efficiency can be expected.

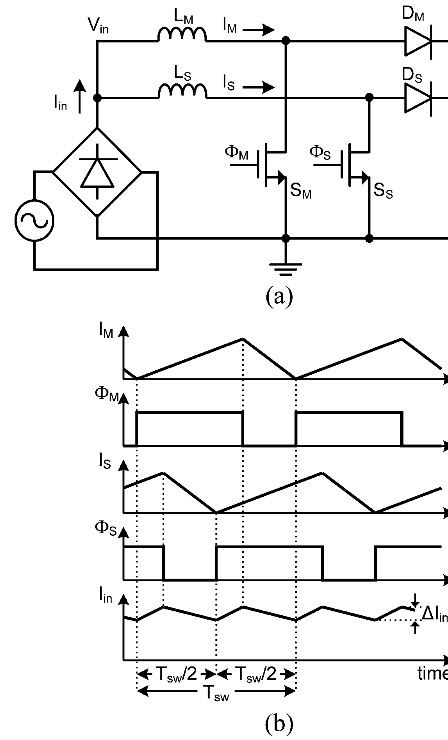

Fig. 1. (a) Two-phase interleaved PFC boost converter and (b) waveforms of a two-phase interleaved CRM PFC converter.

The lower power handling capability of the DCM and CRM can be overcome by paralleling multiple converters [6]. Fig. 1(a) shows a simplified block diagram of a two-phase interleaved PFC boost converter. As shown in Fig. 1(b), if the switching signals Φ_M and Φ_S of the two converters are exactly 180° out of phase, the ripple $\Delta I_{\rm in}$ of the input current can be greatly reduced, which allows smaller input filter. For the DCM and CCM operation, it is easy to generate the switching signals Φ_M and Φ_S spaced by 180° because the switching frequency $f_{\rm sw}$ is fixed. A clock signal whose frequency is $2 \times f_{\rm sw}$ is divided by 2 to get a 50% duty reference clock for switching signal generation. The rising and falling edges of the 50% duty reference clock are

Manuscript received November 21, 2012; revised March 23, 2013; accepted April 26, 2013. Date of current version August 20, 2013. This work was supported by the Samsung Power IC Design (SPID) Center, University of Seoul, Korea, Seoul R&BD under Program SS100022, and Ministry of Science, ICT&Future Planning (MSIP), Korea, under the Information Technology Research Center (ITRC) support program (NIPA-2013-(H0301-13-1013) supervised by the National IT Industry Promotion Agency (NIPA). Recommended for publication by Associate Editor J. A. Cobos.

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Digital Object Identifier 10.1109/TPEL.2013.2262313

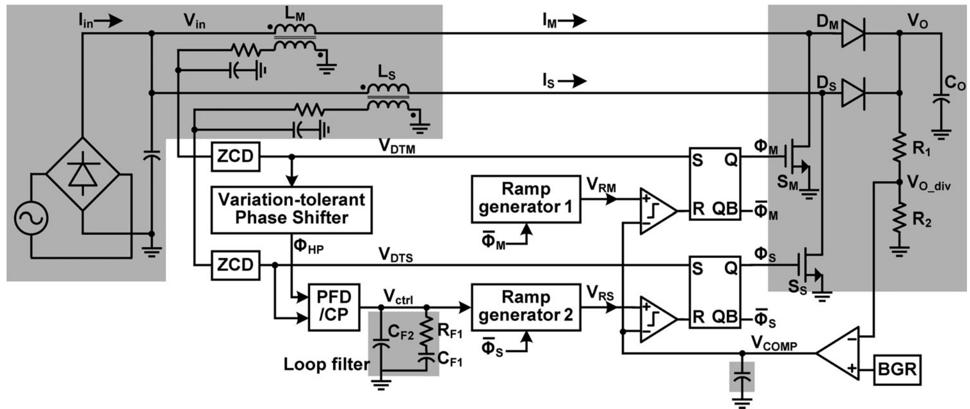


Fig. 2. Two-phase interleaved PFC boost converter with a VTPS. The components in the shaded regions are off-chip.

used to generate the switching signals Φ_M and Φ_S, respectively, while ensuring 180° spacing between them. If a converter operates at the CRM, however, the switching frequency changes according to the instantaneous input line voltage and output current at every switching cycle; therefore, it is impossible to generate the 180° out of phase switching signals by the method explained previously.

For an interleaved power converter operating at the CRM, a master–slave scheme has been widely used [7]–[20]. Among the multiple paralleled converters, a master converter operates as a stand-alone one, while the switching of the other converter, that is, a slave converter, is synchronized with that of the master. For a two-phase interleaved converter, a phase shifter measuring the switching period of the master converter can be used to generate the switching signal of the slave converter, so its switching instant is 180° out of phase from that of the master converter [7]. The simplest way of measuring the switching period of the master converter is to use a ramp generator with UP and DOWN current sources [7]. The mismatch between the two current sources, however, results in the error of the phase shifting, increasing the current ripple ΔI_{in}. A sample-and-hold circuit can be used to measure the period where only one current source is required [8]. The sampling capacitor has to be discharged at every cycle and the time required for this results in phase shifting error.

In this paper, a two-phase PFC boost converter operating at the CRM is described which employs a variation-tolerant phase shifter (VTPS) ensuring the accurate 180° phase shifting. In Section II, the operation principle and circuit implementation of the two-phase PFC boost converter are explained and the stability of the variation-tolerant phase shifting technique is analyzed. The experimental results follow in Section III and the paper is concluded in Section IV.

II. Two-Phase Interleaved CRM PFC Boost Converter With a VTPS

A. Architecture

Fig. 2 shows the block diagram of the two-phase interleaved PFC boost converter with the proposed VTPS operating at the

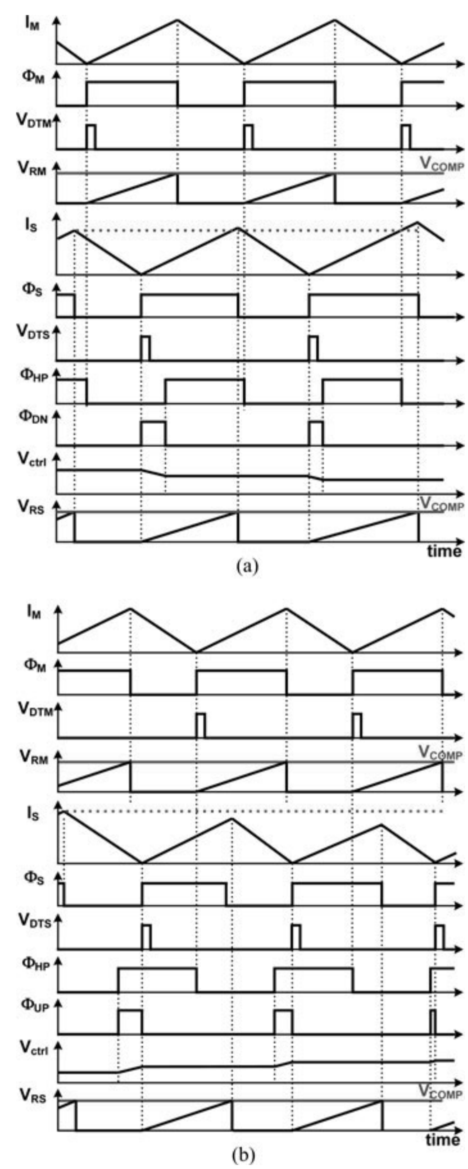
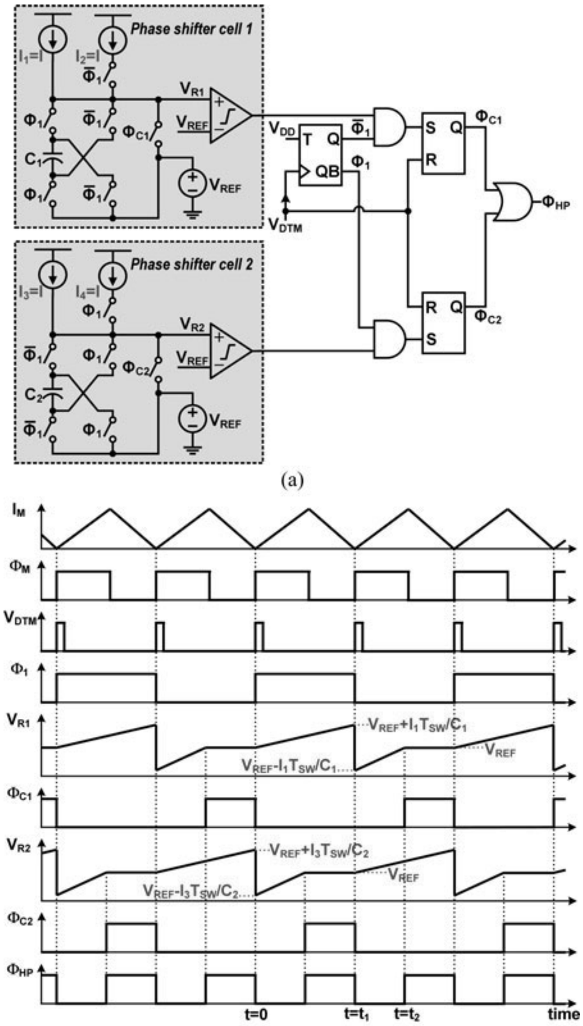


Fig. 3. Timing diagram of the two-phase interleaved CRM PFC boost converter when the slave converter turns ON (a) earlier and (b) later than desired (180° phase shifted from the master converter).



(a)

(b)

Fig. 4. (a) Proposed VTPS and (b) its timing diagram.

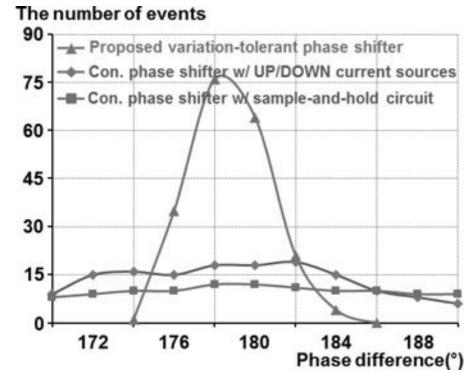


Fig. 5. Monte Carlo simulation result of the three types of phase shifters when the frequency of V_{DTM} is 500 kHz.

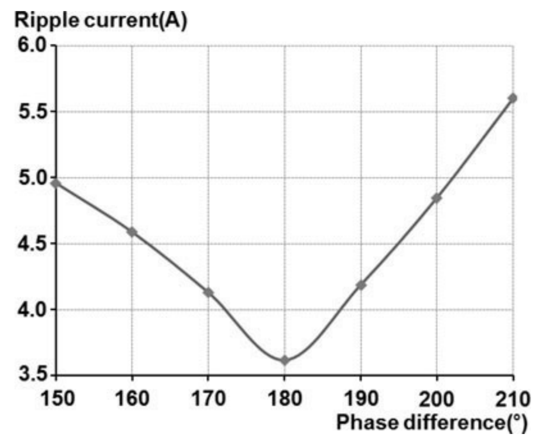


Fig. 6. Simulated input ripple current versus the phase difference between the two converters at the peak of the input line voltage when $V_{\mathrm{in}} = 90\ \mathrm{V_{RMS}}$ and I_{out}=700 mA.

CRM. The upper converter consisting of L_M, D_M, and S_M is the master and the lower one consisting of L_S, D_S, and S_S is the slave. The output voltage level is compared with the reference level generated by the bandgap reference (BGR) to generate the error voltage V_{COMP}. For the master converter, the fixed slope ramp signal V_{RM} is compared with the error voltage V_{COMP} and the switching signal Φ_M becomes LOW when V_{RM} is larger than V_{COMP}, decreasing the inductor current I_M. The voltage level of the secondary winding of the transformers is utilized to detect the zero current of the primary winding. The zero current detector (ZCD) generates the pulse V_{DTM}, setting Φ_M to HIGH when the voltage level of the secondary winding is lower than the reference level.

The operation of the slave converter is similar to that of the master except that the slope of the ramp signal V_{RS} is variable to get the accurate 180° phase difference between the master and slave converters. The slope of V_{RS} is adjusted by the phase shifting loop consisting of the phase-frequency detector (PFD), charge pump (CP), loop filter, and ramp generator, so the rising edge of the ZCD output V_{DTS} of the slave converter is locked to that of Φ_{HP} which is 180° phase shifted from V_{DTM} by the phase shifter. Because the switch S_S of the slave converter is turned ON by the rising edge of V_{DTS}, the turn-ON instant of the slave converter is 180° phase shifted from that of the master converter.

Fig. 3 shows the timing diagram of the two-phase CRM PFC boost converter employing the previously explained phase control scheme. If the slave converter is turned ON earlier (later) than desired, meaning V_{DTS} is faster (slower) than Φ_{HP}, the loop filter output V_{ctrl} controlling the slope of V_{RS} is decreased (increased). Then, the turn-OFF instant of the slave converter becomes slower (faster), which in turn makes the turn-ON instant of the slave converter slower (faster). Because the phase shifting loop locks the rising edge of V_{DTS} to that of Φ_{HP}, the accuracy of the phase shifter is very critical to achieve the desired 180° phase shift between the master and slave converters. The VTPS described below ensures the accurate 180° phase shift.

B. Variation-Tolerant Phase Shifter

Fig. 4(a) shows the proposed VTPS with its timing shown in Fig. 4(b). When the inductor current of the master converter is zero, the ZCD of the master converter generates a short pulse of

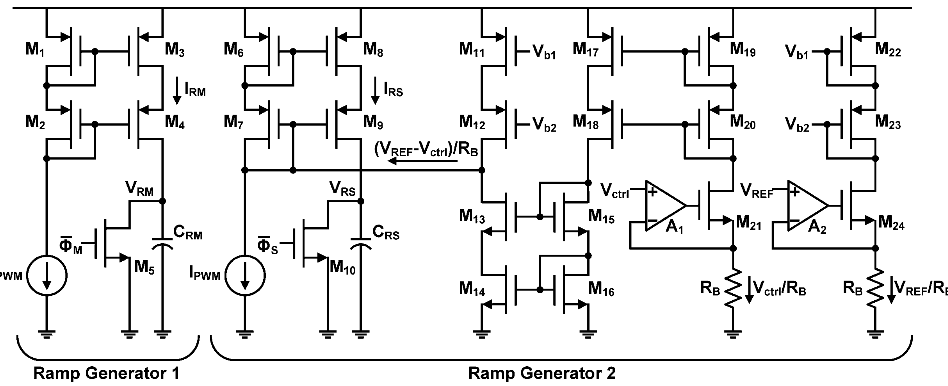


Fig. 7. Ramp generator.

$V_{\rm DTM}$ and the next switching period is started. At this instant, the state of Φ_1 is changed by the toggle flip flop.

When $\Phi_1 =$ LOW and $\Phi_{C1} =$ HIGH, the capacitor C_1 is fully discharged and V_{R1} is initialized to $V_{\rm REF}$. When Φ_1 becomes HIGH at $t = 0$, the capacitor C_1 is now charged by the current source I_1, and V_{R1} is ramped up. At $t = t_1$, the $V_{\rm DTM}$ pulse generated by the ZCD toggles Φ_1 to LOW, which flips the connection of C_1, and V_{R1} is changed to $V_{\rm REF} - (I_1 \cdot T_{{\rm SW},n-1})/C_1$. Because $\Phi_1 =$ LOW and $\Phi_{C1} =$ LOW, C_1 is now charged by the two current sources I_1 and I_2. At $t = t_2$, V_{R1} can be calculated as

$$V_{R1} = V_{\rm REF} - \frac{I_1 \cdot T_{{\rm SW},n-1}}{C_1} + \frac{(I_1 + I_2) \cdot t_2}{C_1} = V_{\rm REF} \quad (1)$$

and t_2 can be rearranged as

$$t_2 = \frac{I_1}{I_1 + I_2} \cdot T_{{\rm SW},n-1} = \frac{1}{2} T_{{\rm SW},n-1}. \quad (2)$$

Since the switching frequency for PFC control changes slowly due to the low bandwidth of the PFC control loop, the previous switching period $T_{{\rm sw},n-1}$ is almost equal to the present switching period $T_{{\rm sw},n}$ and, therefore, t_2 is

$$t_2 = \frac{1}{2} T_{{\rm SW},n}. \quad (3)$$

At $t = t_2$, Φ_{C1} becomes HIGH to set $\Phi_{\rm HP}$, meaning $\Phi_{\rm HP}$ is delayed by 180° from $V_{\rm DTM}$. As explained previously, the phase shifter cell 1 generates $\Phi_{\rm HP}$ delayed by 180° from $V_{\rm DTM}$ when $\Phi_1 =$ LOW. When $\Phi_1 =$ HIGH, Φ_{C2} becomes HIGH by the phase shifter cell 2 to generate $\Phi_{\rm HP}$ delayed by 180° from $V_{\rm DTM}$.

While the conventional phase shifter requires UP and DOWN current sources whose matching is critical but cannot be very good, the proposed one requires only UP current sources, which can be easily matched. A Monte Carlo simulation has been performed to see the achievable accuracy of the phase shift under environmental variations and the results are shown in Fig. 5. The x-axis is the phase difference between the input signal $V_{\rm DTM}$ and the output signal $\Phi_{\rm HP}$; the y-axis represents the number of events. In order to compare the phase shifting accuracy with the conventional ones, the conventional phase shifters with UP and DOWN current sources [7] and with a sample-and-hold circuit [8] are also simulated. As can be seen in the figure, the proposed VTPS shows much better phase shifting accuracy than the others against the environmental variations.

Fig. 6 clearly illustrates the importance of the accurate phase shift between the two converters, where the simulated ripple of the input current at the peak of the input line ac voltage is shown as a function of the phase difference of the two converters for the input line voltage of 90 $\rm V_{RMS}$ and the output current of 700 mA.

C. Ramp Generator

For the proper operation of the interleaved PFC boost converter, the slope of the ramp signal $V_{\rm RS}$ of the slave converter should be adjusted by the loop filter output $V_{\rm ctrl}$. On the contrary, the ramp signal $V_{\rm RM}$ of the master converter has a fixed slope. The ramp generators shown in Fig. 7 provide the required $V_{\rm RM}$ and $V_{\rm RS}$ accordingly. The currents of the transistors M_{21} and M_{24} are given as $V_{\rm ctrl}/R_B$ and $V_{\rm REF}/R_B$, respectively, and are copied to the transistors M_{14} and M_{11}, respectively. Then, the charging current $I_{\rm RS}$ of the ramp generator 2 is $I_{\rm PWM} - (V_{\rm REF} - V_{\rm ctrl})/R_B$. Therefore, the ramp slope of the slave converter increases when the loop filter output $V_{\rm ctrl}$ becomes larger. Because the charging current $I_{\rm RM}$ of the ramp generator 1 is constant, the ramping slope of the master converter is fixed.

D. Stability of the Phase Shifting Loop With the VTPS

In the CRM PFC boost converter, the switching period $t_{\rm sw}$ is the sum of the on-time $t_{\rm on}$ and off-time $t_{\rm off}$ of the switch and is given as

$$t_{\rm sw} = t_{\rm on} + t_{\rm off} = t_{\rm on} + \left(\frac{v_{\rm in}}{v_o - v_{\rm in}}\right) t_{\rm on} = \left(\frac{v_o}{v_o - v_{\rm in}}\right) t_{\rm on} \quad (4)$$

where $v_{\rm in}$ and $v_{\rm out}$ are input and output voltages, respectively. The variables in (4) can be represented as the sum of the dc value and small-signal variation component as

$$\begin{aligned} t_{\rm sw} &= T_{\rm SW} + \hat{t}_{\rm sw} \\ t_{\rm on} &= T_{\rm ON} + \hat{t}_{\rm on} \\ v_o &= V_O + \hat{v}_o \\ v_{\rm in} &= V_{\rm in} + \hat{v}_{\rm in}. \end{aligned} \quad (5)$$

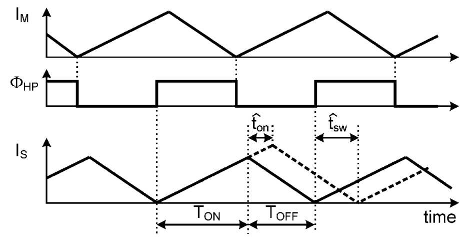


Fig. 8. Perturbation of the switching period when the small on-time perturbation $\hat{t}_{\rm on}$ is induced at the slave converter.

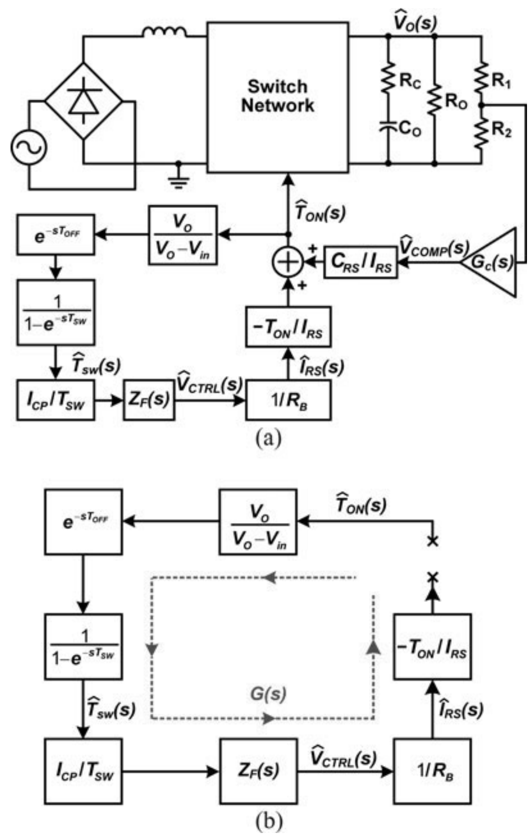


Fig. 9. (a) Small signal model of the slave converter with the VTPS and (b) its open-loop model.

Then, (4) can be rearranged as

$$T_{\rm SW} + \hat{t}_{\rm sw} = \left(\frac{V_O + \hat{v}_o}{V_O + \hat{v}_o - V_{\rm in} - \hat{v}_{\rm in}}\right)\left(T_{\rm ON} + \hat{t}_{\rm on}\right). \quad (6)$$

Assuming $\hat{v}_{\rm in}$ and $\hat{v}_o$ are zero, the aforementioned equation becomes

$$\begin{aligned} T_{\rm SW} + \hat{t}_{\rm sw} &= \left(\frac{V_O}{V_O - V_{\rm in}}\right)\left(T_{\rm ON} + \hat{t}_{\rm on}\right) \\ &= \left(\frac{V_O}{V_O - V_{\rm in}}\right) T_{\rm ON} + \left(\frac{V_O}{V_O - V_{\rm in}}\right)\hat{t}_{\rm on}. \end{aligned} \quad (7)$$

Removing dc values in (7), we obtain the following relationship:

$$\hat{t}_{\rm sw} = \frac{V_O}{V_O - V_{\rm in}}\hat{t}_{\rm on}. \quad (8)$$

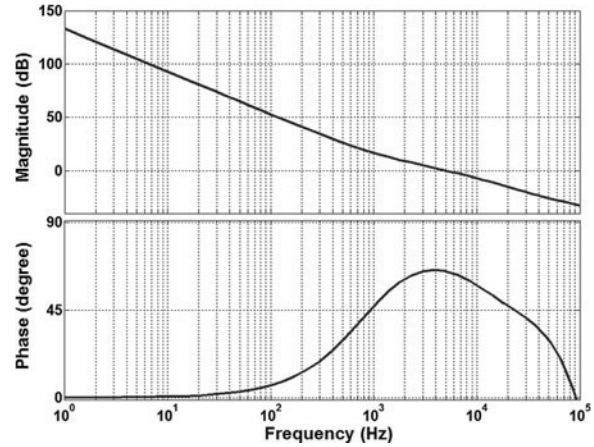


Fig. 10. Open-loop gain and phase of the phase shifting network with the variation tolerant phase shifter when $V_{\rm in} = 90\ \mathrm{V_{RMS}}$ and $I_{\rm out} = 700$ mA.

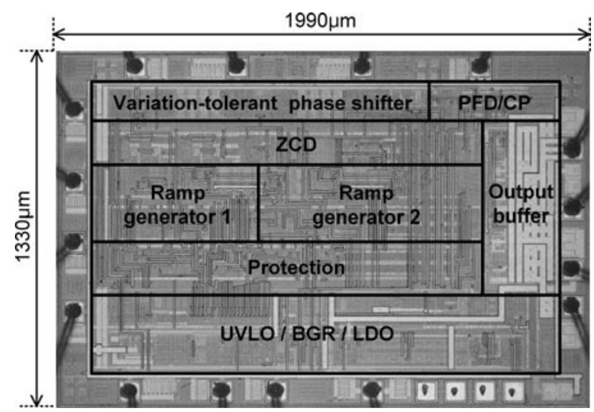


Fig. 11. Microphotograph of the interleaved PFC boost converter with the proposed VTPS.

If there is a variation in the on-time $\hat{t}_{\rm on}$ of the slave converter with the VTPS, the switching period $\hat{t}_{\rm sw}$ would change after some finite delay $T_{\rm OFF}$ as shown in Fig. 8. This can be expressed as [21]

$$\hat{t}_{\rm sw}(t) = \frac{V_O}{V_O - V_{\rm in}}\hat{t}_{\rm on}(t)\cdot\delta(t - T_{\rm OFF}). \quad (9)$$

Therefore, $\hat{t}_{\rm sw}$ of the nth cycle is the sum of the $\hat{t}_{\rm sw}$ of the $(n$–1)th cycle and the variation due to the change in the on-time $\hat{t}_{\rm on}$, which can be represented as

$$\hat{t}_{{\rm sw},n}(t) = \hat{t}_{{\rm sw},n-1}(t) + \hat{t}_{{\rm on},n}(t)\cdot\left(\frac{V_O}{V_O - V_{\rm in}}\right)\cdot\delta(t - T_{\rm OFF}). \quad (10)$$

Taking the Laplace transformation of (10), we obtain

$$\begin{aligned} &\hat{T}_{{\rm SW},n}(s) - \hat{T}_{{\rm SW},n}(s)\cdot e^{-sT_{\rm SW}} \\ &\quad = \hat{T}_{{\rm ON},n}(s)\cdot\left(\frac{V_O}{V_O - V_{\rm in}}\right)\cdot e^{-sT_{\rm OFF}}. \end{aligned} \quad (11)$$

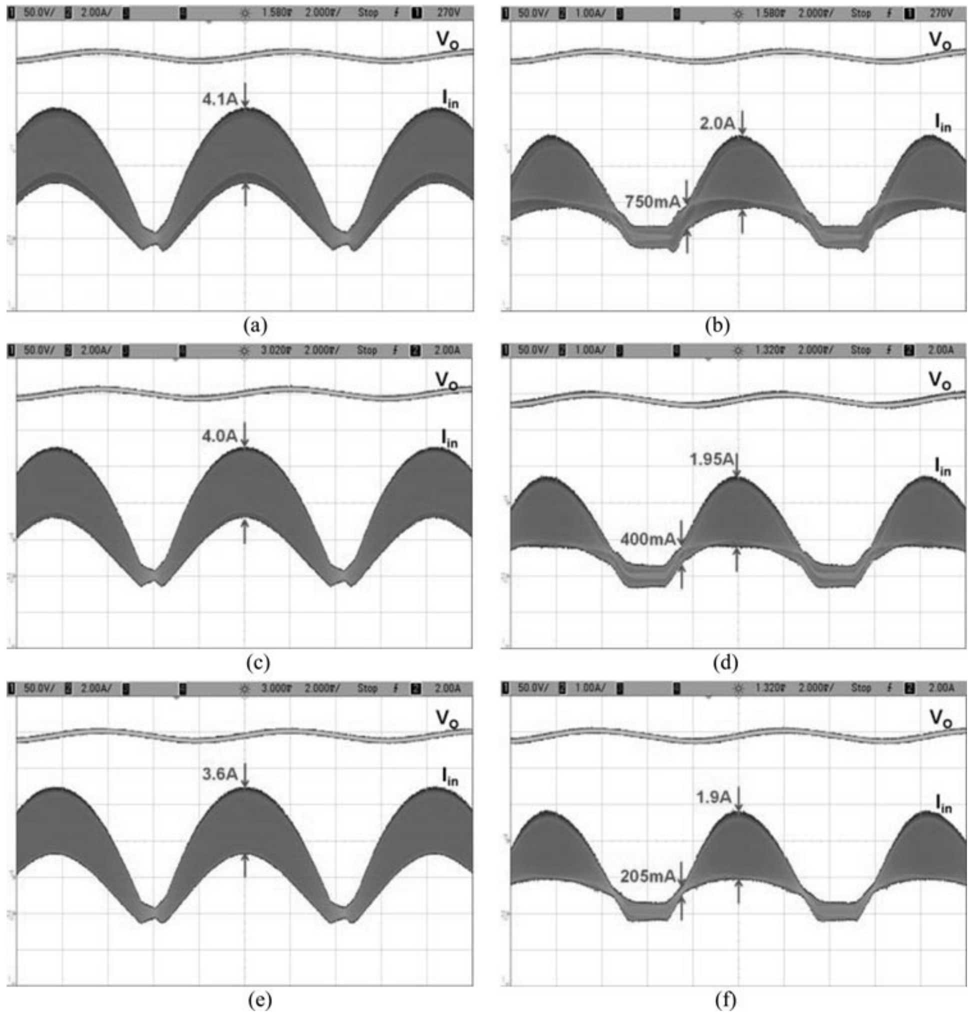


Fig. 12. Measured waveforms of the PFC boost converter output V_O and input current $I_{\rm in}$ at $I_{\rm out} = 700$ mA with the conventional phase shifter with UP/DOWN current sources for (a) $V_{\rm in} = 90\ \rm V_{RMS}$ and (b) $V_{\rm in} = 264\ \rm V_{RMS}$, with the conventional phase shifter with sample and hold circuit for (c) $V_{\rm in} = 90\ \rm V_{RMS}$ and (d) $V_{\rm in} = 264\ \rm V_{RMS}$, and with the proposed phase shifter for (e) $V_{\rm in} = 90\ \rm V_{RMS}$ and (f) $V_{\rm in} = 264\ \rm V_{RMS}$.

Therefore, the transfer function $\hat{T}_{\rm SW}(s)/\hat{T}_{\rm ON}(s)$ is

$$\frac{\hat{T}_{\rm SW}(s)}{\hat{T}_{\rm ON}(s)} = \frac{\hat{T}_{{\rm SW},n}(s)}{\hat{T}_{{\rm ON},n}(s)} = \frac{1}{1-e^{-sT_{\rm SW}}}\cdot\left(\frac{V_O}{V_O - V_{\rm in}}\right)\cdot e^{-sT_{\rm OFF}}. \tag{12}$$

When the switching period changes, the PFD and CP generate the pumping current for $\hat{t}_{\rm sw}$ and the loop filter output is given as

$$\hat{V}_{\rm CTRL}(s) = I_{\rm CP}\cdot\frac{\hat{T}_{\rm SW}(s)}{T_{\rm SW}}\cdot Z_F(s) \tag{13}$$

where $Z_F(s)$ is the impedance of the loop filter. The variation of the loop filter output changes the charging current $I_{\rm RS}$ of the slave ramp signal generator as shown in Fig. 7. Because the charging current $I_{\rm RS}$ is $I_{\rm PWM}$–($V_{\rm REF}$–$V_{\rm ctrl}$)/R_B, the variation of the charging current $I_{\rm RS}$ can be written as

$$\hat{i}_{\rm rs} = \frac{\hat{v}_{\rm ctrl}}{R_B}. \tag{14}$$

and by the Laplace transformation

$$\hat{I}_{\rm RS}(s) = \frac{\hat{V}_{\rm CTRL}(s)}{R_B}. \tag{15}$$

The variation of the charging current $I_{\rm RS}$ of the ramp generator changes the on-time as

$$T_{\rm ON} + \hat{t}_{\rm on} = \frac{V_{\rm COMP}\cdot C_{\rm RS}}{I_{\rm RS} + \hat{i}_{\rm rs}} \tag{16}$$

which can be rearranged as

$$T_{\rm ON}I_{\rm RS} + T_{\rm ON}\hat{i}_{\rm rs} + I_{\rm RS}\hat{t}_{\rm on} + \hat{t}_{\rm on}\hat{i}_{\rm rs} = V_{\rm COMP}C_{\rm RS}. \tag{17}$$

The last term of the left part of (17) can be neglected, and because $T_{\rm ON} = V_{\rm COMP}C_{\rm RS}/I_{\rm RS}$,

$$T_{\rm ON}\hat{i}_{\rm rs} + I_{\rm RS}\hat{t}_{\rm on} = 0. \tag{18}$$

Therefore, the transfer function $\hat{T}_{\rm ON}(s)/\hat{I}_{\rm RS}(s)$ can be obtained as

$$\frac{\hat{T}_{\rm ON}(s)}{\hat{I}_{\rm RS}(s)} = -\frac{T_{\rm ON}}{I_{\rm RS}}. \tag{19}$$

From the aforementioned observations, the small signal model of the phase shifting loop with the VTPS can be obtained as shown in Fig. 9(a) Because the crossover frequency of the voltage regulation loop of the PFC converter is very low,

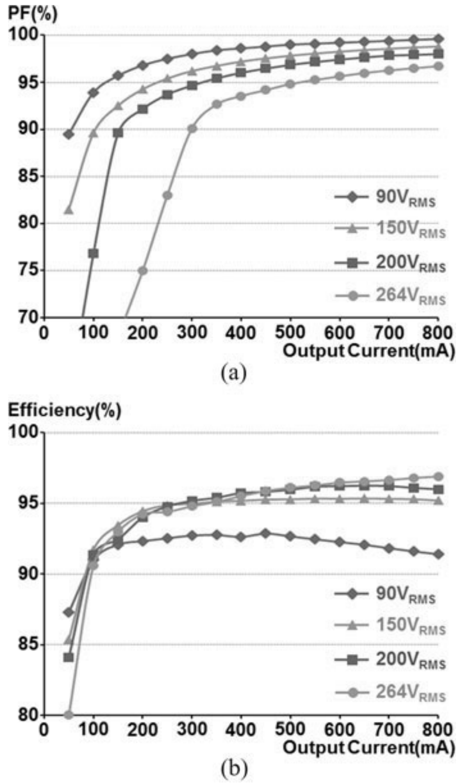


Fig. 13. Measured PF and efficiency of the PFC boost converter with the proposed VTPS.

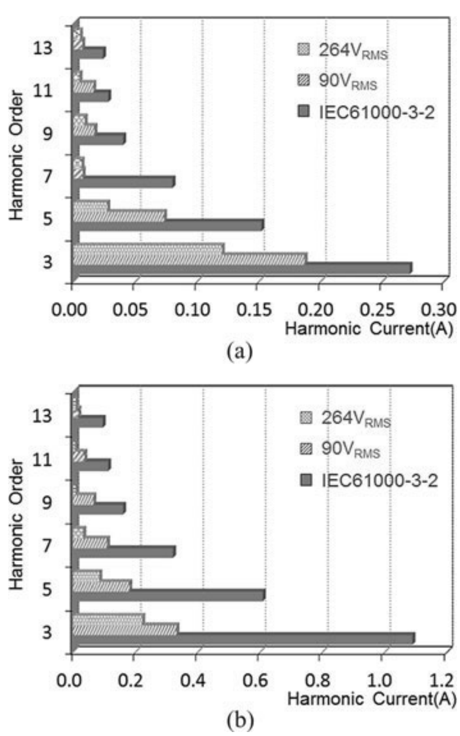


Fig. 14. Measured harmonics current and IEC61000-3-2 Class D specification at (a) $I_{\rm out} = 200$ mA and (b) $I_{\rm out} = 800$ mA.

the output voltage of the PFC converter and, therefore, the error voltage $V_{\rm COMP}$ can be considered to be constant. Then, the open-loop transfer function of the phase shifting network with

TABLE I
PERFORMANCE SUMMARY

Parameter	Value	Unit	Condition
Technology	0.35-μm BCDMOS process		
Operating mode	CRM		-
Input line voltage	90~264	V_{RMS}	AC
Output voltage	393	V	DC
Inductor value	160	μH	
Capacitor value	164	μF	
MOSFET	TK13A60D		
Diode	SFF1008G		
Minimum suppotable switching freqneucy	25	kHz	Frequency limitation of the phase shifter
Supply voltage	10~25	V	-
Reference voltage	3.7	V	-
Internal supply	5	V	Linear regulator output
Maximum output current	800	mA	Maximum output power : 320-W
Output buffer rising time	75	nsec	Load capacitance : 2-nF
Output buffer falling time	91	nsec	
Current consumption	6	mA	Excluding driving current of power switch
Quiescent current	0.12	mA	-

the VTPS shown in Fig. 9(b) is

$$G(s) = -\left(\frac{V_O}{V_O - V_{\rm in}}\right) \cdot e^{-sT_{\rm OFF}} \cdot \frac{1}{1 - e^{-sT_{\rm SW}}} \cdot \frac{I_{\rm CP}}{T_{\rm SW}} \cdot \frac{Z_F(s)}{R_B} \cdot \frac{T_{\rm ON}}{I_{\rm RS}}. \quad (20)$$

The magnitude and phase of the open-loop transfer function $G(s)$ are shown in Fig. 10 when the input line voltage and output current are 90 $V_{\rm RMS}$ and 700 mA, respectively. The crossover frequency of the phase shifting loop is about 5 kHz and the phase margin is 67°, which means the phase shifting network is stable.

III. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed VTPS, three types of two-phase interleaved CRM PFC boost converter providing 320 W maximum output power have been implemented in a 0.35-μm BCDMOS process. The three converters have the same circuitry except the phase shifting network. Two of them have the conventional phase shifter, that is, the conventional one with the UP and DOWN current sources [7] and the one with the sample-and-hold circuit [8]. The third one has the proposed VTPS. Among the three converters, Fig. 11 shows the microphotograph of the one with the proposed phase shifter. The area of the whole chip is 2.65 mm^2 where the proposed phase shifter occupies 0.14 mm^2.

Fig. 12 shows the measured waveforms of the PFC output V_O and the input current I_{in} with the three types of phase shifters under different line conditions. As shown in the figure, the PFC boost converter with the proposed phase shifter shows the lowest input current ripple because the proposed variation-tolerant phase shifter provides the most accurate 180° phase shift.

The PFC boost converter provides 393-V dc output from the ac input line voltage of 90–264 V_{RMS}. The maximum output current is 800 mA, while 6 mA is dissipated internally for the operation of the interleaved PFC controller excluding the driving current of power switch. In Fig. 13, the PF and power efficiency of the PFC boost converter are shown for the input line voltage of 90, 150, 200, and 264 V_{RMS} with the proposed VTPS. The harmonics of the current are measured for the input line voltage of 90 and 264 V_{RMS} and the results are shown in Fig. 14(a) and (b) when the output current is 200 and 800 mA, respectively. The harmonics are lower than the IEC 61000-3-2 Class-D specifications.

The performance of the PFC boost converter employing the proposed VTPS is summarized in Table I.

IV. Conclusion

For a two-phase interleaved PFC converter, a variation-tolerant 180° phase shifter has been developed and applied to a 320-W CRM PFC boost converter implemented in a 0.35-μm BCDMOS process. The input current ripple can be greatly reduced with the proposed phase shifter compared with the conventional phase shifting techniques. Although the proposed phase shifter has been applied to a PFC boost converter, it can be used in any type of two-phase interleaved switching power converter.

Acknowledgment

The authors would like to thank Prof. J. Choi of University of Seoul, Korea, for his continuous support of this work. The CAD tools were provided by the IC Design Education Center, Korea.

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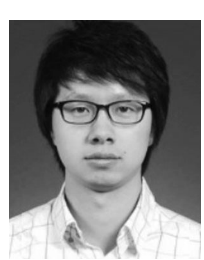

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