A Novel Bidirectional Multilevel Boost-Buck Dc-Dc Converter

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***Abstract* -- A novel noninverting boost-buck dc-dc converter topology is presented, applicable when both sides of the converter need to have the same grounding. It is based on the back-to-back connection of two *n*-level diode-clamped converter legs, and allows bidirectional power flow. A simplified topology is proposed for unidirectional power flow applications. Two new pulse width modulation strategies with different advantages are proposed to operate the converter guaranteeing dc-link capacitor voltage balance in every switching cycle for all possible operating conditions and using small capacitance values. The semiconductor device losses are analytically compared to the losses in a conventional two-level boost-buck converter. The analysis yields a higher efficiency for the multilevel converter, especially as the number of levels increases. Experimental results are presented to validate the good converter performance in a five-level converter prototype.**

***Index Terms*—Dc-dc power conversion, multilevel systems, pulse width modulated power converters, pulse width modulation.**

I. INTRODUCTION

Buck-boost or boost-buck dc-dc converters are required in applications with an output voltage level within an input voltage range. For instance, in battery powered systems (e.g., in portable equipments) where the battery voltage might be higher or lower than the desired output voltage depending on the battery charge state. Other applications include the interfacing of dc energy sources such as photovoltaic panels [1] and thermoelectric generators [2], dc-dc converters for telecom power supplies [3], connection of battery powered dc buses with different voltage levels (requires bidirectional power flow), etc. In general, the potential applications present a wide range of power and voltage levels. Additionally, the step-down (buck) and step-up (boost) voltage capabilities of these converters make them usable in most dc-dc conversion applications.

The conventional topology for the noninverting buck-boost (boost-buck) converter is made up of a cascaded connection of a two-level buck (boost) converter and a two-level boost (buck) converter. In [4], two new topologies are proposed employing lower-voltage-rated devices to improve the efficiency of the converter. A different approach to benefit from the better economical and performance features of lower-voltage-rated devices operating at lower blocking voltage levels is to use a multilevel converter. In [5]-[6] capacitor-clamped topologies are used for buck dc-dc conversion applications. In [7], the use of a three-level neutral-point-clamped leg is introduced in dc-dc converters with galvanic isolation. However, so far no diode-clamped topologies have been reported in dc-dc power conversion with the same grounding for the input and output sides, except for the three-level topology employed in [8], which is derived from a three-level neutral-point-clamped converter leg.

This paper explores the possibility and benefits of using *n*-level diode-clamped topologies in dc-dc conversion applications. In Section II, a bidirectional boost-buck dc-dc converter topology made up of two diode-clamped *n*-level converter legs is proposed. A simplified topology for unidirectional power flow applications is also presented. Section III defines two possible pulsewidth modulation (PWM) strategies and proposes a closed-loop balancing control to maintain the dc-link capacitor voltages balanced in every switching cycle. Section IV analyzes the possible reduction in semiconductor device losses as compared to a conventional two-level converter. Section V presents experimental results verifying the good performance of the proposed converter and Section VI outlines the conclusions.

II. CONVERTER TOPOLOGY

Fig. 1 shows the elementary topologies for noninverting and bidirectional dc-dc conversion with both buck and boost operating modes. They are derived from the cascaded connection of a two-level buck (boost) converter and a two-level boost (buck) converter. The circuit in Fig. 1(b) presents two inductors and a capacitor vs. only one inductor in Fig. 1(a). However, Fig. 1(a) presents pulsating (non-continuous) input and output currents i_a and i_b which will usually require the introduction of capacitance at the input and output terminals of the converter, whereas these currents are continuous in Fig. 1(b).

The proposed dc-dc converter topology, which is the multilevel extension of Fig. 1(b), made up of two back-to-back connected diode-clamped converter legs, is shown in Fig. 2. A dc source/load is connected at terminals *A* and 1, and a dc load/source is connected at terminals *B* and 1. A converter made up of a single leg is not considered because

This work was supported by the Ministerio de Educación y Ciencia, Madrid, Spain, under Grants TEC2005-08042 and TEC2008-01794.

the dc-link capacitor voltages cannot be balanced in this case [5], except for the particular three-level topology described in [8]. As can be seen, the topology is symmetric, allowing power flow in both directions and any positive value of $m = V_B / V_A$ (buck and boost operating modes possible).

In unidirectional power flow applications, the topology can be simplified by removing half of the switches and half of the anti-parallel diodes of each leg. Additionally, we can further simplify the topology by removing half of the clamping diodes as shown in Fig. 3.

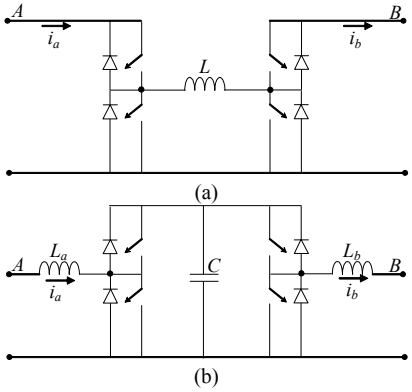

Fig. 1. Basic bidirectional dc-dc converters with buck and boost operating modes. (a) Buck-boost topology. (b) Boost-buck topology.

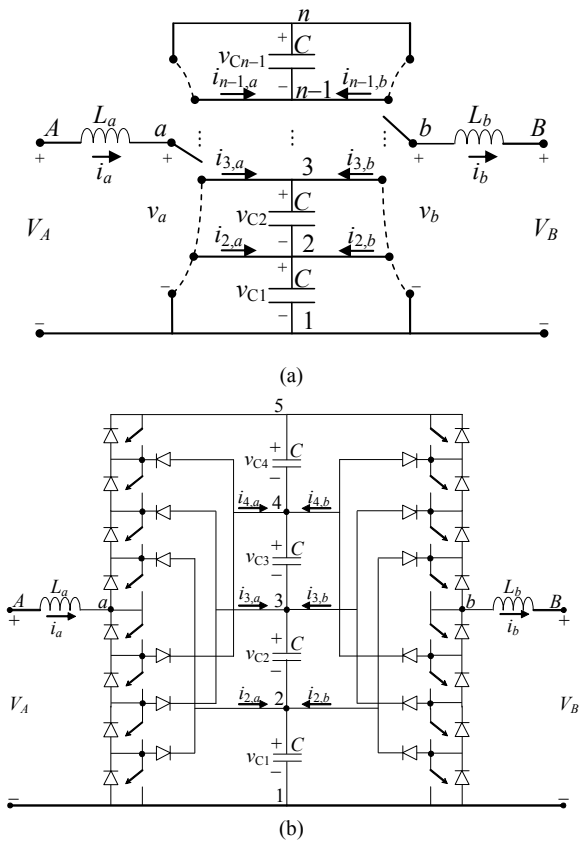

Fig. 2. Multilevel diode-clamped dc-dc converters. (a) Functional diagram of an n-level converter. (b) Five-level converter topology.

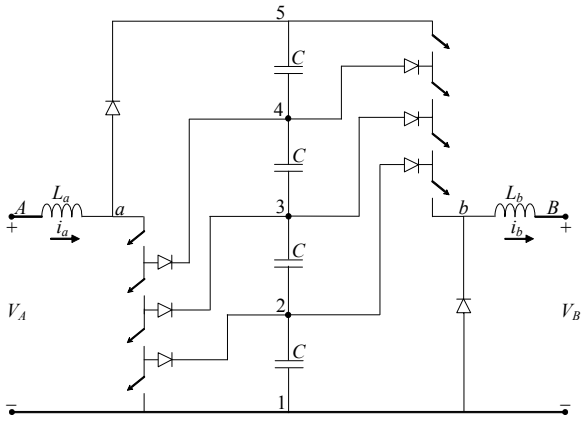

Fig. 3. Simplified five-level topology in unidirectional power flow applications (i_a, $i_b > 0$).

III. Pulsewidth Modulation and Capacitor Voltage Balance Control

Two pulsewidth modulation (PWM) strategies have been derived for the proposed converter. The converter legs are operated in a quasi-two-level mode similar to what has been proposed in [9] for dc-ac multilevel diode-clamped three-phase converters and, additionally, the dc-link capacitor voltage balance is guaranteed in every switching cycle.

The PWM strategies are defined in terms of variables d_{xy}, which represent the duty ratio of the connection of the output leg terminal x ($\in\{a, b\}$) to the dc-link point y ($\in\{1, 2,\ldots,n\}$) in a given switching cycle. It will be assumed that $V_A > V_B$. If $V_A < V_B$, we just need to swap the defined duty ratios of legs a and b, due to the symmetry of the topology. To guarantee capacitor voltage balance under high current ripple, unequal switching behavior, etc., these PWM strategies are combined with the closed-loop balancing control presented in [10] (in particular, with perturbation scheme A).

There are three conditions that must be met by both modulations strategies. First of all, to guarantee the dc-link capacitor voltage balance in every switching cycle, the average current in every switching cycle injected into the inner dc-link points ($i_{j,a}+i_{j,b} = d_{aj}\cdot i_a - d_{bj}\cdot i_b$, $j\in\{2, 3,\ldots,n-1\}$) must be zero. Assuming a lossless converter ($V_A\cdot I_a = V_B\cdot I_b$), this condition can be expressed as

$$d_{bj} = m\cdot d_{aj};\quad j\in\{2,3,\ldots,n-1\}. \tag{1}$$

Second, in steady state and assuming capacitor voltage balanced operation

$$\begin{aligned} V_A &= \sum_{j=2}^{n}\left[d_{aj}\cdot(j-1)\frac{V_n}{n-1}\right] \\ V_B &= \sum_{j=2}^{n}\left[d_{bj}\cdot(j-1)\frac{V_n}{n-1}\right], \end{aligned} \tag{2}$$

where V_n ($= v_{C1}+v_{C2}+\ldots+v_{C(n-1)}$) is the total dc-link voltage.

Third, the leg duty-ratios must verify

$$\sum_{j=1}^{n} d_{aj} = 1;\quad \sum_{j=1}^{n} d_{bj} = 1. \tag{3}$$

A. PWM Scheme 1

To minimize the number of switching transitions in leg *a* and the value of the total dc-link voltage V_n

$$d_{a1} = 0. \tag{4}$$

All leg duty-ratios of connection to the inner dc-link points are set to the same value, to have the same margin for capacitor voltage balance regulation

$$d_{a2}, d_{a3}, \cdots, d_{a(n-1)} = \delta, \tag{5}$$

where δ (>0) is a user-defined parameter.

From (3)-(5)

$$d_{an} = 1 - (n-2)\cdot\delta. \tag{6}$$

Combining (1) and (5)

$$d_{b2}, d_{b3}, \cdots, d_{b(n-1)} = m\cdot\delta. \tag{7}$$

From (2) and (5)-(7)

$$d_{bn} = m\cdot[1-(n-2)\cdot\delta] \tag{8}$$

Finally, from (3), (7), and (8)

$$d_{b1} = 1 - m. \tag{9}$$

Therefore, PWM Scheme 1 is defined by (4)-(9)

$$\begin{aligned} &d_{a1} = 0 \\ &d_{a2}, d_{a3}, \cdots, d_{a(n-1)} = \delta \\ &d_{an} = 1-(n-2)\cdot\delta \\ &d_{b1} = 1-m \\ &d_{b2}, d_{b3}, \cdots, d_{b(n-1)} = m\cdot\delta \\ &d_{bn} = m\cdot[1-(n-2)\cdot\delta] \end{aligned} \tag{10}$$

Provided that currents i_a and i_b are approximately constant over the switching cycle, this PWM scheme guarantees capacitor voltage balance in every switching cycle. As mentioned earlier, to guarantee capacitor voltage balance under high current ripple, unequal switching behaviour, etc., this PWM scheme is combined with the balancing control presented in [10] (in particular, with perturbation scheme A) applied to leg *b*. The value of the dc-link voltage V_n and the maximum value of δ are

$$\begin{aligned} V_n &= \frac{2\cdot V_A}{2-(n-2)\cdot\delta} \\ \delta_{\max} &= \frac{1}{n-1}. \end{aligned} \tag{11}$$

On one hand, it is interesting to have a small value of δ to decrease the value of V_n and hence reduce the device blocking voltage and switching losses. On the other hand, it is interesting to increase its value to have more dc-link capacitor voltage balancing margin [10]. A tradeoff has to be made.

B. PWM Scheme 2

An alternative PWM strategy is defined by

$$\begin{aligned} &d_{a1}, d_{a2}, \cdots, d_{a(n-1)} = \delta \\ &d_{an} = 1-(n-1)\cdot\delta \\ &d_{b1} = 1-m\cdot(1-\delta) \\ &d_{b2}, d_{b3}, \cdots, d_{b(n-1)} = m\cdot\delta \\ &d_{bn} = m\cdot[1-(n-1)\cdot\delta] \end{aligned} \tag{12}$$

In this case, the value of V_n and the maximum value of δ are

$$\begin{aligned} V_n &= \frac{2\cdot V_A}{2-n\cdot\delta} \\ \delta_{\max} &= \frac{1}{n}. \end{aligned} \tag{13}$$

This PWM scheme presents a higher number of switching transitions and a higher value of V_n than PWM scheme 1, but it has more margin to regulate the dc-link capacitor voltages because the balancing control [10] can be applied to both converter legs *a* and *b*, and it allows the integration of the gate-driver power supplies within the power device die for all devices of the two converter legs [11], [12].

IV. Semiconductor Device Loss Analysis

A discussion follows regarding the comparison of semiconductor device losses in the conventional two-level and the proposed *n*-level boost-buck converters. The comparison is made for the same terminal voltages V_A and V_B, the same constant (negligible ripple) terminal currents I_a and I_b, with $I_a = m\cdot I_b$. We will further assume that $V_A > V_B$, without loss of generality due to the symmetry of the topology.

Assuming a similar value of the conduction voltage drop per rated voltage for all semiconductor devices, conduction losses should be similar in both cases. The main difference in device losses will be due to the different switching pattern. The next two subsections explore the difference in switching and reverse recovery losses.

A. Switching Losses

For each converter leg, switching transitions occur in pairs: one switch turns off and one switch turns on. To simplify the analysis, it is initially assumed that diodes are ideal (lossless) and that the losses are concentrated in either the controlled device turning on or the device turning off, according to the pattern described in Fig. 4, where $v_s(t)$ and $i_s(t)$ are the voltage across the switch and the current through the switch, respectively. The absolute values of the voltage and current slopes during transitions are assumed to be constant and equal to s_v and s_i, regardless of the value of V_s and I_s. With these assumptions, the energy lost in a switching transition of an *n*-level converter leg is

$$E_s = \frac{V_n^2\cdot I_s}{2\cdot(n-1)^2\cdot s_v} + \frac{V_n\cdot I_s^2}{2\cdot(n-1)\cdot s_i}. \tag{14}$$

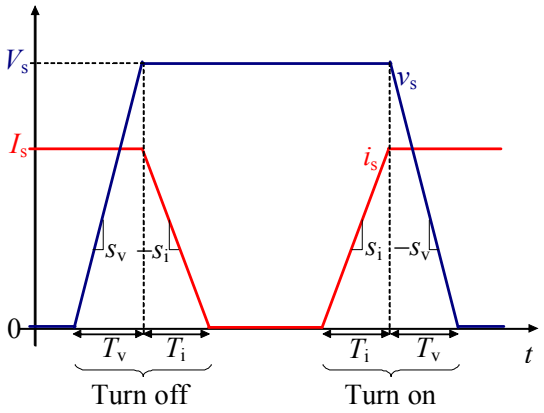

Fig. 4. Voltage and current waveforms during switching transitions in the controlled devices concentrating the switching losses.

Let us additionally assume that $s_v/s_i = k \cdot V_A/I_b$; i.e., the voltage and current transition times (T_v and T_i) are equal for $V_s = k \cdot V_A$ and $I_s = I_b$. The comparison is initially made assuming that leg a of the two-level converter is not switching; i. e., the high-side switch of leg a is permanently on and the low-side switch is off. This is the less favorable case for the multilevel ($n \geq 3$) converter, since in this converter both legs are switching, according to (10) and (12).

The ratio of the switching losses per switching-cycle in leg b of the multilevel converter ($E_{Ts,b,n}$) with regard to the switching losses in leg b of the two-level converter ($E_{Ts,b,2}$) can be computed as

$$\frac{E_{Ts,b,n}}{E_{Ts,b,2}} = \frac{4 + 2 \cdot k \cdot (n-1) \cdot (2 - (n-2) \cdot \delta)}{(1+k) \cdot (n-1) \cdot (2 - (n-2) \cdot \delta)^2} \quad \text{(PWM 1)}$$
$$\frac{E_{Ts,b,n}}{E_{Ts,b,2}} = \frac{4 + 2 \cdot k \cdot (n-1) \cdot (2 - n \cdot \delta)}{(1+k) \cdot (n-1) \cdot (2 - n \cdot \delta)^2} \quad \text{(PWM 2)}. \qquad (15)$$

Fig. 5 shows this ratio for $\delta = 0.01$ and several values of k. It can be observed that, for low values of δ, the multilevel converter produces lower losses in leg b than the two-level converter, especially as n increases and k decreases. The results are similar for both PWM schemes.

The ratio of total switching losses in both legs a and b of the multilevel converter ($E_{Ts,ab,n} = E_{Ts,a,n} + E_{Ts,b,n}$), with reference to the same losses in the two-level converter ($E_{Ts,ab,2}$), can be computed as

$$\frac{E_{Ts,ab,n}}{E_{Ts,ab,2}} = \frac{2}{(1+k) \cdot (n-1)^2 \cdot (2 - (n-2) \cdot \delta)^2} \cdot \left[\begin{array}{l} 2 \cdot \left[(1+m) \cdot (n-1) - m \right] + \\ + k \cdot (n-1) \cdot (2 - (n-2) \cdot \delta) \cdot \left[(1+m^2) \cdot (n-1) - m^2 \right] \end{array} \right] \quad \text{(PWM 1)}$$
$$\frac{E_{Ts,ab,n}}{E_{Ts,ab,2}} = \frac{4 \cdot (1+m) + 2k \cdot (n-1) \cdot (2 - n \cdot \delta) \cdot (1+m^2)}{(1+k) \cdot (n-1) \cdot (2 - n \cdot \delta)^2} \quad \text{(PWM 2)}. \qquad (16)$$

Fig. 6 shows this ratio as a function of m and for several values of n and k. The ratio increases as m approaches 1. The multilevel converter presents lower overall switching losses for all the range of variable m for values of n high enough and values of k low enough.

The results in Figs. 5 and 6 assume that only one leg in the two-level converter is switching. To avoid small duty-ratio values of the switch control signals when $m \approx 1$ or for other design purposes, it may be interesting to operate the two-level converter with both legs switching. In this case, the switching losses of the multilevel converter will be clearly lower. Fig. 7 shows the ratio of the total losses as a function of n for a case where the two-level converter is operated with the same duty ratio for the boost and buck converter stages, $m \approx 1$, producing a voltage $V_n = 2 \cdot V_A$. The multilevel converter is operated with PWM scheme 2 and $\delta = 1/n$ to produce the same V_n value. The ratio of losses in this case can be computed as

$$\frac{E_{Ts,ab,n}}{E_{Ts,ab,2}} = \frac{2 + k \cdot (n-1)}{(2+k) \cdot (n-1)} \quad \text{(PWM 2)}. \qquad (17)$$

Further reduction of the ratio of losses in Figs. 5-7 can be expected if the low-voltage-rated devices of the multilevel converter can operate with higher values of s_v and s_i than the devices of the two-level converter.

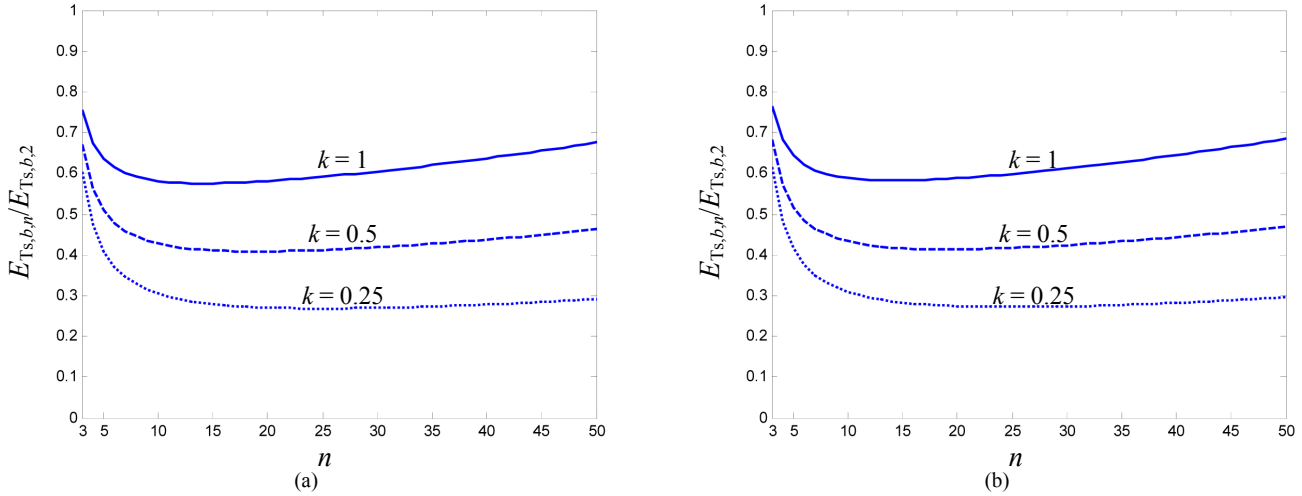

Fig. 5. Ratio of the switching losses in leg b as a function of the number of levels n, for $\delta = 0.01$. (a) PWM scheme 1. (b) PWM scheme 2.

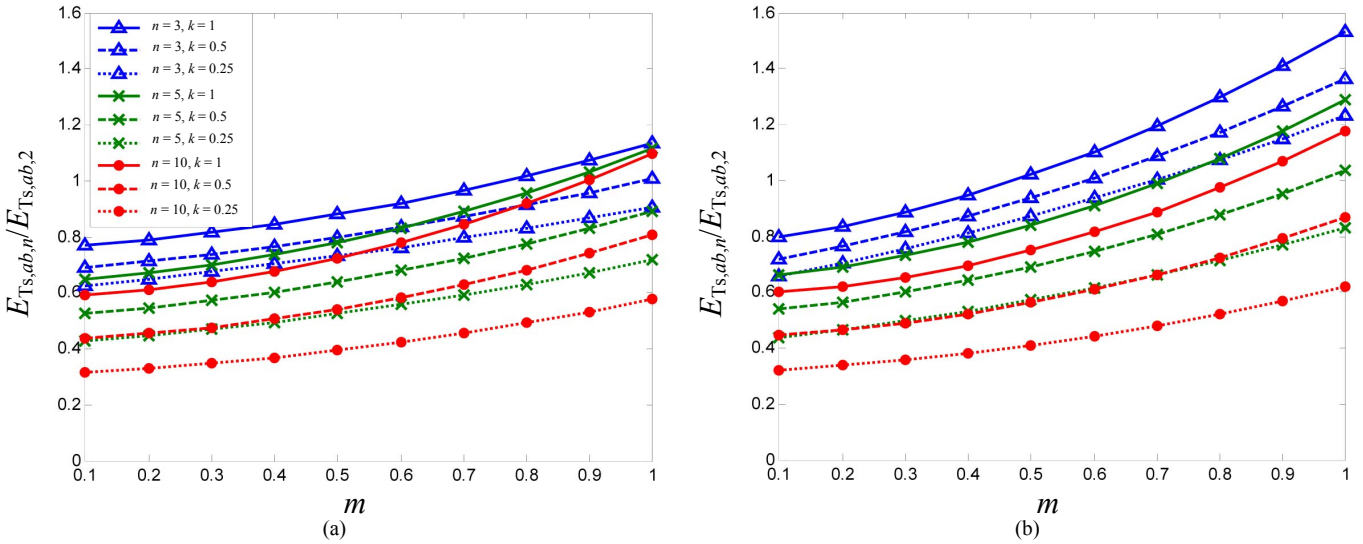

Fig. 6. Ratio of the total switching losses in legs *a* and *b* as a function of *m*, for δ = 0.01. (a) PWM scheme 1. (b) PWM scheme 2.

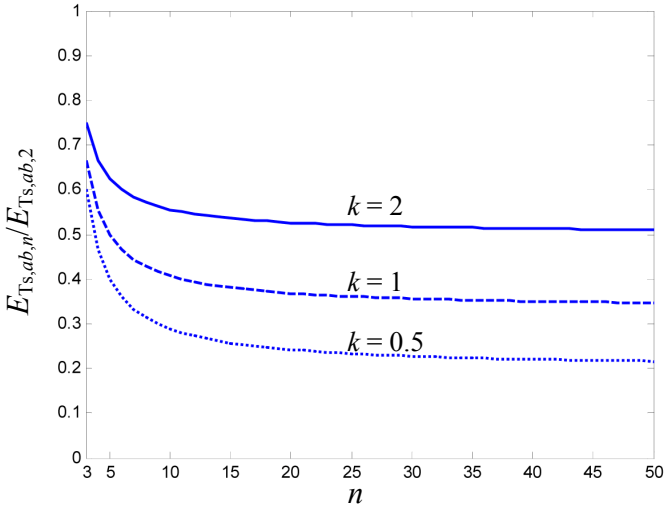

Fig. 7. Ratio of the total switching losses in legs *a* and *b* as a function of *n*. Conditions: $m \approx 1$, both legs of the two-level converter switching, $V_n = 2 \cdot V_A$, and the multilevel converter operated with PWM scheme 2 and $\delta = 1/n$.

B. Reverse Recovery Losses

Reverse recovery losses occur when a conducting diode turns off and recovers a reverse-biased operating point [13]. The reverse recovery current produces losses not only in the diode but especially in the corresponding switch turning-on and supplying the reverse recovery current. The total energy loss can be roughly estimated as

$$E_{rr} = V_{Db} \cdot (Q_{rr} + t_a \cdot I), \tag{18}$$

where V_{Db} is the device (diode and switch) blocking voltage, I is the diode and switch conducting current, and Q_{rr} is the reverse recovery charge, which is a function of the diode rated voltage (V_{Dr}) (or diode technology), V_{Db}, I, and s_i. This charge is the addition of the minority carriers that must be removed from the diode p-n junction and the charges required to build up the blocking voltage across the effective capacitance of the depletion layer. Variable t_a is the time elapsed from the point in time where the diode conducts a zero current until it reaches the peak reverse recovery current, which is a function of V_{Dr} , I, and s_i.

In a two level converter, only one diode conducts and produces reverse recovery losses per leg and per switching cycle. These losses are

$$E_{Trr,2} = V_n \cdot \left[Q_{rr}(V_{Dr}, V_n, I, s_i) + t_a(V_{Dr}, I, s_i) \cdot I \right] \tag{19}$$

To study the multilevel ($n \geq 3$) converter case, the diode-clamped topology presented in [14] is assumed, where all diodes have a blocking voltage equal to $V_n/(n-1)$. In this topology, and assuming PWM scheme 2, $(n-1) \cdot n/2$ diodes conduct per leg in every switching cycle. They conduct in $n-1$ groups of 1, 2, …, and $n-1$ series-connected diodes. Each group of series-connected diodes turns off against the turn on of a switch with blocking voltage $V_n/(n-1)$ supplying the reverse recovery current to remove the minority carriers in the p-n junctions. Only one diode in the group immediately recovers its blocking voltage. Therefore, the reverse recovery losses in this transition are equivalent to the full reverse recovery losses of a two-level converter with blocking voltage $V_n/(n-1)$. The remaining diodes will only produce reverse recovery losses through the current required to charge the effective capacitance of their depletion layer when they recover their blocking voltage. Assuming these losses to recharge the effective capacitance negligible, the per-leg and per-switching-cycle total reverse recovery energy loss in a multilevel converter is

$$E_{Trr,n} = (n-1) \cdot \frac{V_n}{n-1} \cdot \left[\begin{array}{l} Q_{rr}\left(\frac{V_{Dr}}{n-1}, \frac{V_n}{n-1}, I, s_i \right) + \\ + t_a\left(\frac{V_{Dr}}{n-1}, I, s_i \right) \cdot I \end{array} \right]. \tag{20}$$

If both the two-level and multilevel converters operate

with the same dc-link voltage V_n, it can be reasonably expected that

$$Q_{\mathrm{rr}}\left(V_{\mathrm{Dr}}, V_n, I, s_{\mathrm{i}}\right) > Q_{\mathrm{rr}}\left(\frac{V_{\mathrm{Dr}}}{n-1}, \frac{V_n}{n-1}, I, s_{\mathrm{i}}\right)$$
$$t_{\mathrm{a}}\left(V_{\mathrm{Dr}}, I, s_{\mathrm{i}}\right) > t_{\mathrm{a}}\left(\frac{V_{\mathrm{Dr}}}{n-1}, I, s_{\mathrm{i}}\right). \quad (21)$$

Therefore, the total reverse recovery losses in the multilevel converter can be expected to be lower than in the two-level converter.

V. Experimental Results

Figs. 9 and 10 present experimental results obtained with the setup shown in Fig. 8. A five-level converter prototype with 150 V metal oxide semiconductor field effect transistors (MOSFETs) has been used. The two PWM schemes are tested under buck and boost operating modes. The computation of the 8 independent leg duty-ratios is performed by the embedded PowerPC of dSpace DS1103. This information is sent to an Altera EPF10K70 programmable logic device in charge of generating the 16 switch control signals. It is interesting to note that the dc-link capacitor voltages remain balanced, despite of the significant current ripple.

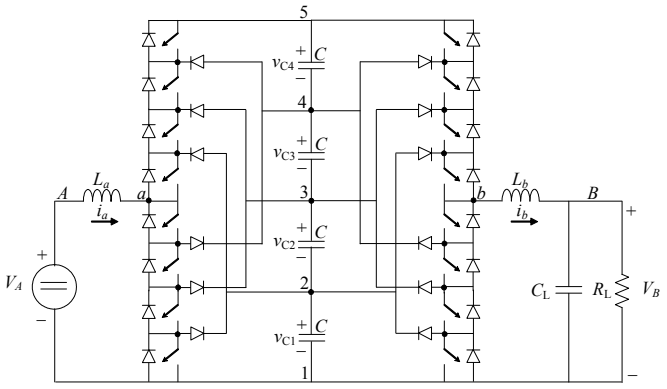

Fig. 8. Experimental setup.

VI. Conclusion

A novel multilevel noninverting boost-buck dc-dc converter topology has been presented. The topology is applicable when both sides of the converter need to have the same grounding. It consists of the back-to-back connection of two *n*-level diode-clamped converter legs. Two new PWM strategies with different advantages have been proposed to operate the converter guaranteeing dc-link capacitor voltage balance in every switching cycle and using small capacitance values. According to the analysis presented, the overall converter efficiency can be expected to be higher than in the conventional two-level boost-buck converter because of the use of lower voltage rated devices with better performance features and also operated at lower blocking voltage values.

If a particular switch (e.g., MOSFET), ideally with integrated auxiliary circuitry (gate driver, gate-driver power supply, protections…), and a particular diode (e.g., Schottky), both with good performance characteristics, are available; then, multilevel converters of different voltage ratings could be built from these two devices. The extended use of these two devices could bring their cost down enough to make the proposed multilevel topologies competitive with conventional topologies.

The converter symmetry, buck and boost capabilities, bidirectional power flow, good efficiency and low cost from using selected optimal cost and performance devices, and continuous input and output currents, make this converter a possible candidate for a universal, easily scalable dc-dc converter topology to be used in a number of different applications.

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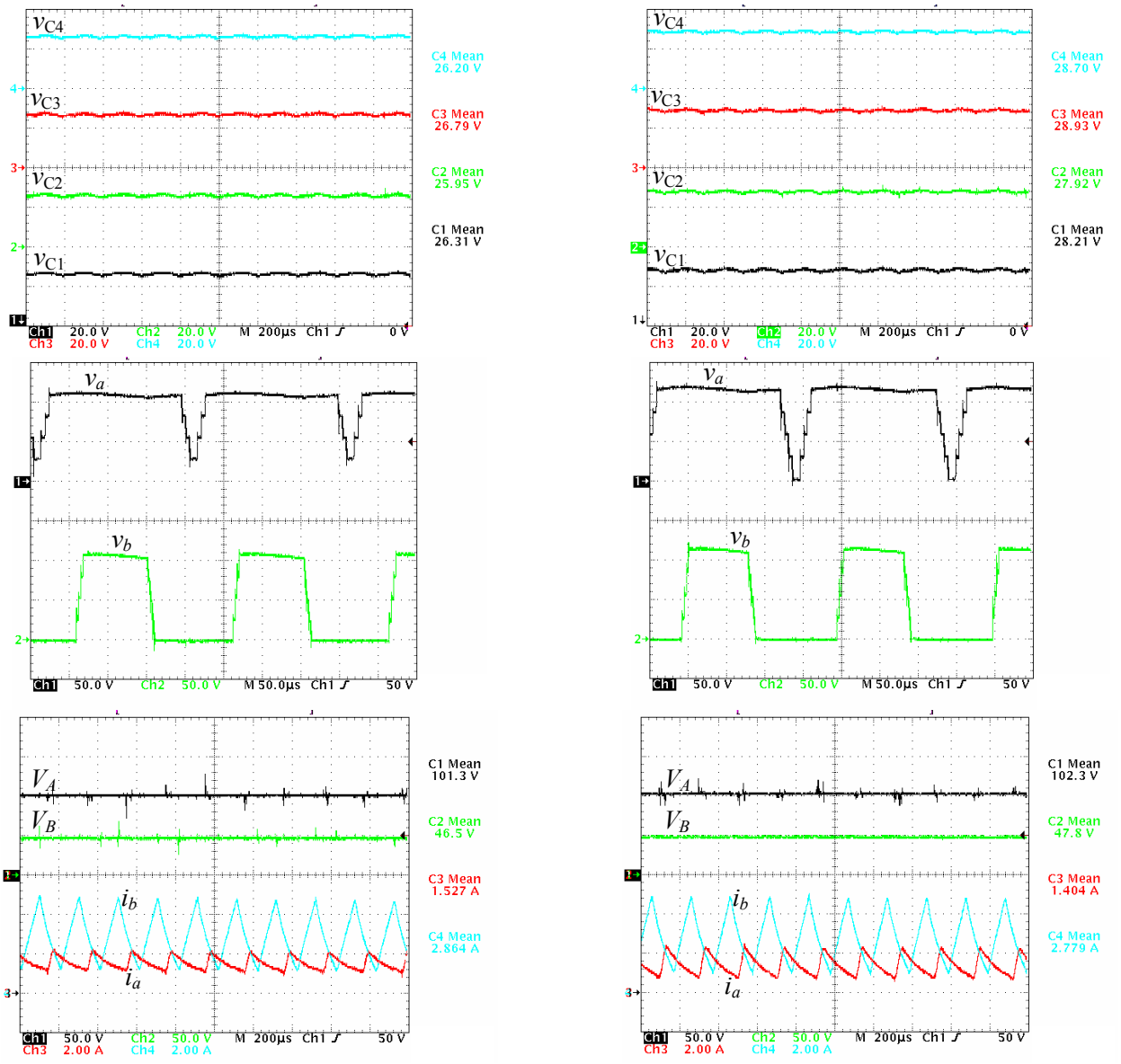
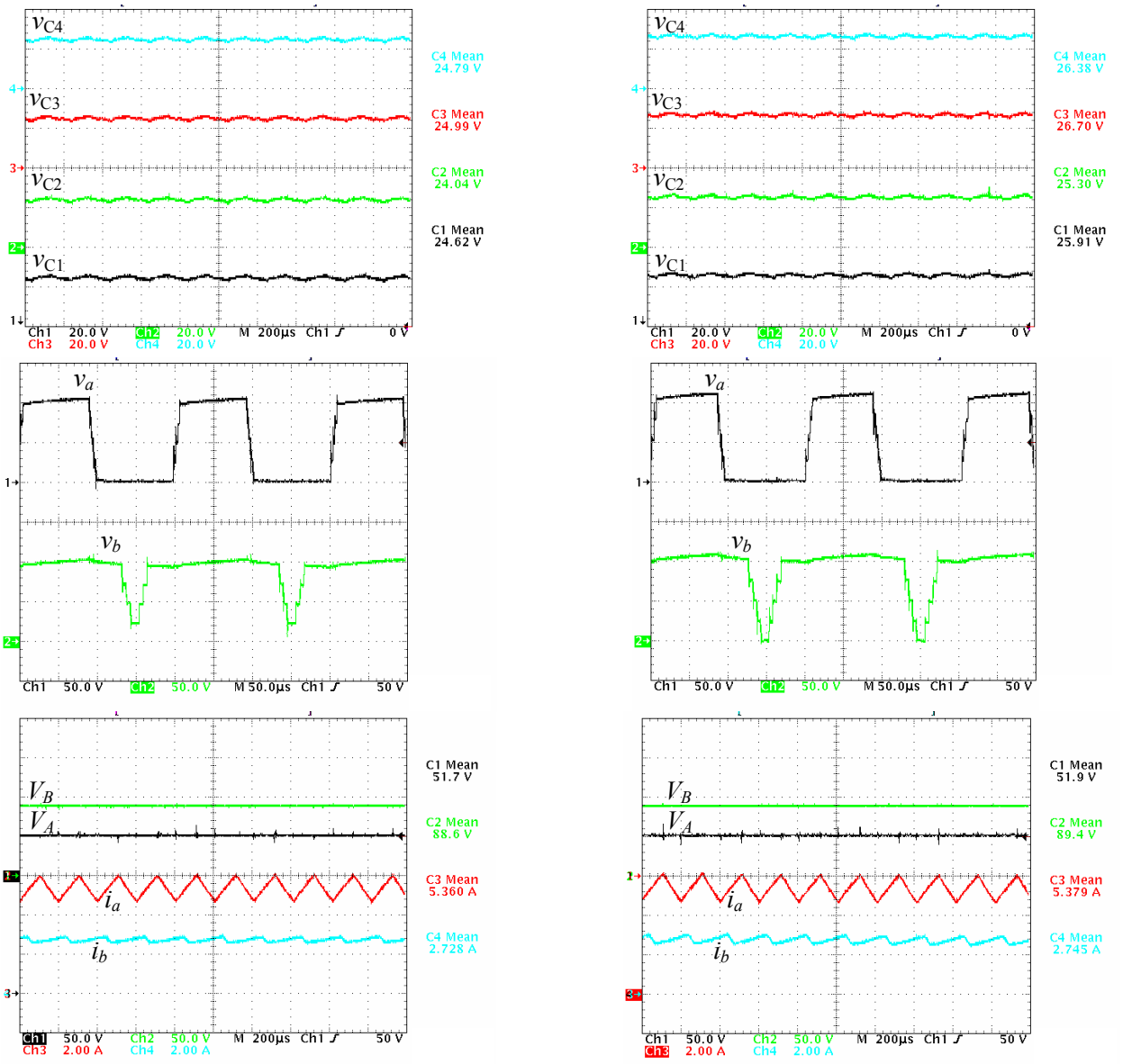


(a) (b)

Fig. 9. Experimental results for v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_a, v_b, V_A, V_B, i_a, and i_b with the setup shown in Fig. 8 and in the following conditions: prototype built with 150 V MOSFETs, $m = 0.5$, $V_A = 100$ V, $C = 155$ µF, $L_a = L_b = 2.5$ mH, $R_L = 16{,}5$ Ω, $C_L = 470$ µF, switching frequency $f_s = 5$ kHz, $\delta = 0.05$, no output voltage regulation, and with the closed-loop balancing control of [10]. (a) PWM scheme 1. (b) PWM scheme 2.



(a) (b)

Fig. 10. Experimental results for v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_a, v_b, V_A, V_B, i_a, and i_b with the setup shown in Fig. 8 and in the following conditions: prototype built with 150 V MOSFETs, $m = 2$, $V_A = 50$ V, $C = 155$ µF, $L_a = L_b = 2.5$ mH, $R_L = 33$ Ω, $C_L = 470$ µF, switching frequency $f_s = 5$ kHz, $\delta = 0.05$, no output voltage regulation, and with the closed-loop balancing control of [10]. (a) PWM scheme 1. (b) PWM scheme 2.