Buck / Boost Dc – Dc Converter Topology with Soft Switching in Whole Operating Region.

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Abstract – The paper proposes a buck/boost dc-dc converter topology based on the principle of auxiliary resonant commutated pole. The used snubber is fairly simple yet effective in reducing the switching losses. All active devices operate with soft switching and switching noise is suppressed as much as possible. In addition to the conventional active switch loss reduction, the snubber participates in suppression of output diode reverse recovery. Moreover, complete soft switching in the whole operating region is achieved through controlled extended reverse conduction of synchronous rectifier. The topology was implemented in a 14 kW converter prototype operating at 62.5 kHz and tested with complete closed loop control. Experimental efficiencies in the range of 98.5 % show that the proposed circuit is highly capable while remaining sufficiently simple.

***Index Terms* — soft switching, dc-dc converter, high-efficiency, buck-boost topology**

I. INTRODUCTION

Since the main operating principles of basic power converters were well understood, attaining high efficiency and power density are among the core priorities of research in power electronics. The two goals are often coupled since it is infeasible to reach high power densities in converters with excessive losses. Power loss is most often reduced by using various soft switching methods.

One of the soft switching methods frequently used in dc-dc buck/boost converters employs so-called active snubbers [1] – [7]. Through their use, Zero Voltage Transition (ZVT) [1] respectively Zero Current Transition (ZCT) [2] are obtained during the main semiconductor turn-on process, turn-off process or both and the switching losses are significantly reduced. This approach was shown to be very effective and dc-dc converters with 99 % efficiency using auxiliary snubber principles were recently reported [3].

In spite of excellent performance of converters employing active snubbers in terms of efficiency and power density [3], they are often considered too complex for practical application [4] – [9]. Certain complexity must be justifiable since active snubbers always require additional components to attain ZVT respectively ZCT. However, too much complexity often results in intricate spatial layout and complex timing constraints. Due to such factors, designers are often reluctant to using converters with active snubbers in spite of their excellent control of switching performance.

In order to deal with complexity of active snubber-based dc-dc buck/boost converters, a topology employing a simple snubber shown in Figure 1 was proposed in [10]. This topology is based on Auxiliary Resonant Commutated Pole (ARCP) snubber concept introduced in [11] to soft switched inverters. The application of such snubber to inverters is renowned and discussed in literature [11], [12], [13]; however, its application to dc-dc converters is rare. The advantage of this snubber is that it offers soft switching without a significant increase of main device stresses unlike some other topologies [6] – [8], [14]. In addition, its use in dc-dc buck/boost topology enables soft switching in the whole operating region irrespective of the load.

In spite of all the benefits, the topology proposed in [10] and shown in Figure 1 has also a problem with voltage spike across the auxiliary bidirectional switch. In order to suppress this spike, a modified auxiliary circuit is proposed in this paper, resulting in the circuit shown in Figure 2. The modifications consist of snubber capacitors added in parallel to auxiliary diodes and of a saturable inductor added in the

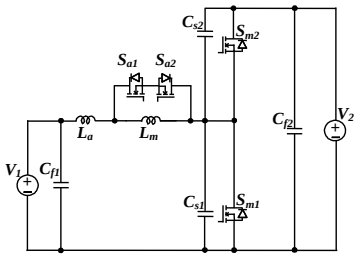


Figure 1. Circuit diagram of forward boost reverse buck dc-dc converter with simple snubber [10]

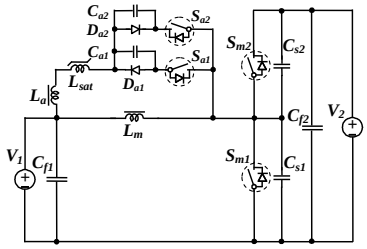


Figure 2. Modified two quadrant forward boost reverse buck topology

auxiliary current path. The modified snubber successfully suppresses the voltage spike, resulting in smooth and noiseless waveforms also in the auxiliary circuit.

In addition to the above mentioned circuit modifications, this paper also introduces a so-called hybrid operating mode which allows for complete soft switching at low loads as well as at zero load. Timing requirements for closed loop control are also discussed and the paper is concluded by full power experiments on the converter prototype.

II. Circuit Topology

The proposed circuit operates in three main operating modes: Forward Boost Mode (FBM), Reverse Buck Mode (RBM) and Bidirectional Hybrid Mode (BHM). Operating cycle of each of these modes can be further subdivided into distinct time intervals in order to better describe the converter operation. There are many similarities between the individual time intervals in all three main operating modes and therefore similar time intervals are discussed together in order to avoid repeated description of common operating principles. Table I shows the naming scheme used in the following paragraphs.

A. Forward Boost and Reverse Buck Operation

One switching cycle in forward boost and reverse buck mode may be subdivided into eleven time intervals as shown in Figure 3 and Figure 4. Auxiliary current pulse is formed during Intervals F1 to F7 and Intervals R1 to R7 respectively. These are discussed in detail in paragraph 0C. Once the auxiliary pulse intervals are over, the operation continues by main circuit intervals shown in Figure 5 and discussed below.

1) ***Interval F9 and R9*** *– $t_6<t<t_7$ – Storing Energy in Main Inductor L_m (Figure 5a)*

This interval is a standard interval present in conventional hard switched converters. The main current flows from the energy source through the main inductor L_m and the main switch. Main energy portion is stored in L_m during this interval. Duration of this interval defines the difference between the output and input voltage. The duration is often controlled by the voltage controller and the interval ends by turning *off* the main switch.

2) ***Interval F10 and R10*** *– $t_7<t<t_8$ – ZVS turn-off of Main Switch (Figure 5b)*

When the main switch turns *off*, the current I_{Lm} commutates almost instantly to the capacitors C_{s1} and C_{s2}. These capacitors serve as turn-off snubber slowing down the voltage change across the main switches, effectively resulting in ZVS turn-off. The snubber capacitors are charged / discharged by the main current. The interval ends when the charge/discharge cycle is completed. In that moment, the main diode turns *on* and the next interval begins.

The auxiliary switch is turned *off* during Interval F9/R9. The turn-off is with ZCS and the voltage difference across the auxiliary switch is equal to zero during the whole Interval F9/R9. Therefore, the parasitic output capacitance of the auxiliary switch only starts charging when the main switch

TABLE I. Naming Scheme Used in Discussion of Operating Intervals

	FBM Boost Aux. pulse	RBM Buck Aux. pulse
Main Switch	S_{m1}	S_{m2}
Main Diode	S_{m2}	S_{m1}
Aux. Switch	S_{a1}	S_{a2}
Aux. Diode	D_{a1}	D_{a2}
Aux. Snubber Capacitor	C_{a1}	C_{a2}

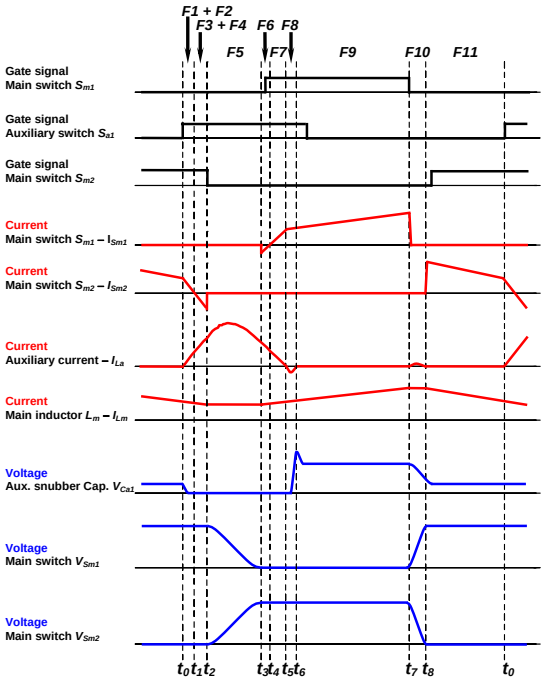


Figure 3. Basic waveforms in forward boost operation

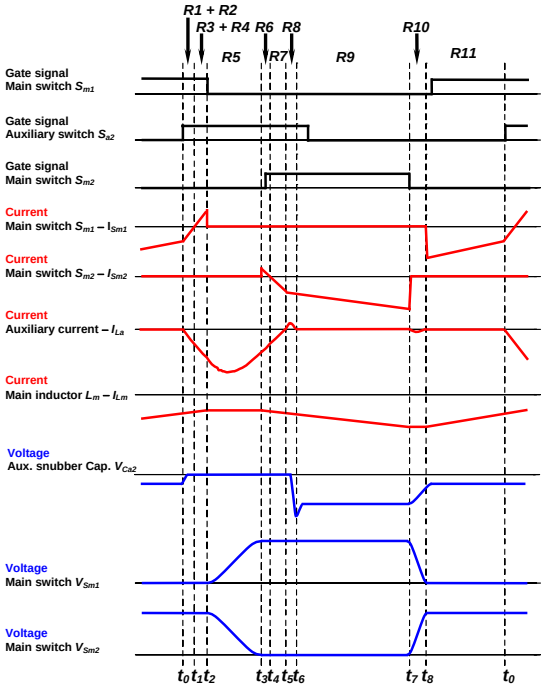


Figure 4. Basic waveforms in reverse buck operation

turns *off* at the beginning of Interval F10/R10. The charging of this capacitance also discharges the auxiliary snubber capacitor. The discharge ends when the voltage of the output capacitance of the auxiliary switch is fully charged. The final voltage of the auxiliary snubber capacitor depends primarily on the ratio between its capacitance and the output capacitance of the auxiliary switch as well as on the difference between the input and output voltage. This final voltage is often clamped to zero by the auxiliary diode.

3) ***Interval F11 and R11*** *– $t_8<t<t_0$ – Transferring Energy to Load Side (Figure 5c)*

Interval F11/R11 is another of the standard hard switched operating modes. It begins by the main current commutating from the snubber capacitors to the main diode. After a short while, making sure that the main switch is completely *off* and the whole main current has commutated to the main diode, the switch in parallel to the main diode may be turned *on* to enable synchronous rectification (SR). This action "removes" the current from the body diode into the MOSFET channel which reduces the conduction losses as well as reverse recovery of the main diode when it switches *off* in Interval F3/R3. During this interval a part of the energy stored in the main inductor L_m is transferred to the output. The interval ends by turning *on* the auxiliary switch and the switching cycle continues by the first auxiliary pulse interval F1/R1.

B. Hybrid Operation

Hybrid operating mode is used at low power levels when the current flowing though the main inductor at the moment of turn-off of the main switch is not high enough to maintain ZVS. A typical example is no load case when most of the soft switched topologies loose the soft switching ability. The proposed circuit uses two auxiliary current pulses to maintain soft switching even at zero load current.

The hybrid mode can be subdivided into fourteen time intervals as indicated in Figure 6. Intervals H1 to H5 are used to form the boost auxiliary pulse in order to achieve smooth transition of the common point between S_{m1} and S_{m2} from zero to V_2. Reversed transition from V_2 to zero is managed by the buck auxiliary current pulse formed during intervals H8 to H12. Both auxiliary pulses are discussed in detail in paragraph 0C. Main circuit modes which do not involve auxiliary pulses are shown in Figure 7 and discussed below.

1) ***Interval H6 + H7*** *– $t_4<t<t_6$ – Main Current Through L_m Increasing $dI > 0$ (Figure 7a)*

During Interval H6, the current of inductor L_m is steadily rising from its minimum value. The rate of the current rise dI can be calculated as V_1/L_m. In the time instant t_5, the current seamlessly crosses though zero and Interval H7 begins. This interval differs from H6 only in the reversed direction of the main inductor current. The interval ends by turning *on* the auxiliary switch S_{a2} which initiates the buck auxiliary pulse.

2) ***Interval H13 + H14*** *– $t_4<t<t_6$ – Main Current Through L_m Decreasing $dI < 0$ (Figure 7b)*

Interval H13 follows upon completion of the buck auxiliary pulse. During this interval, the current of the main

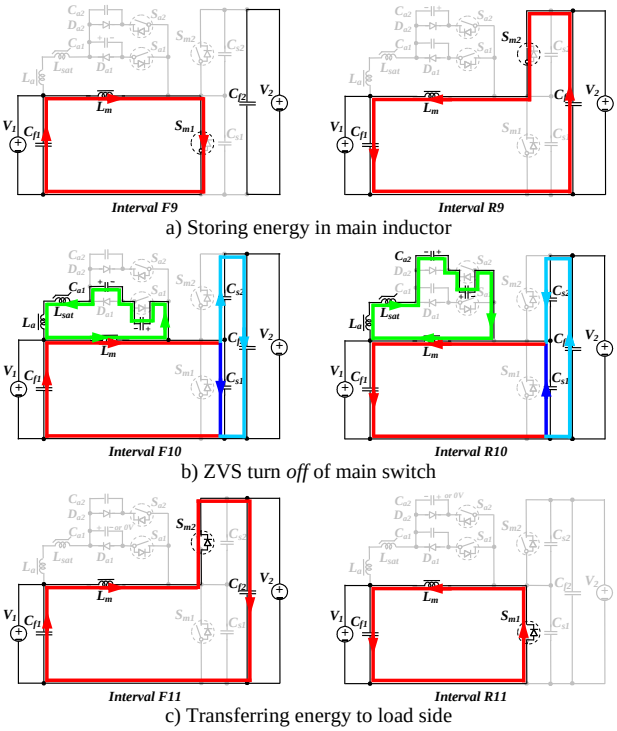


Figure 5. Main circuit intervals in boost and buck operation

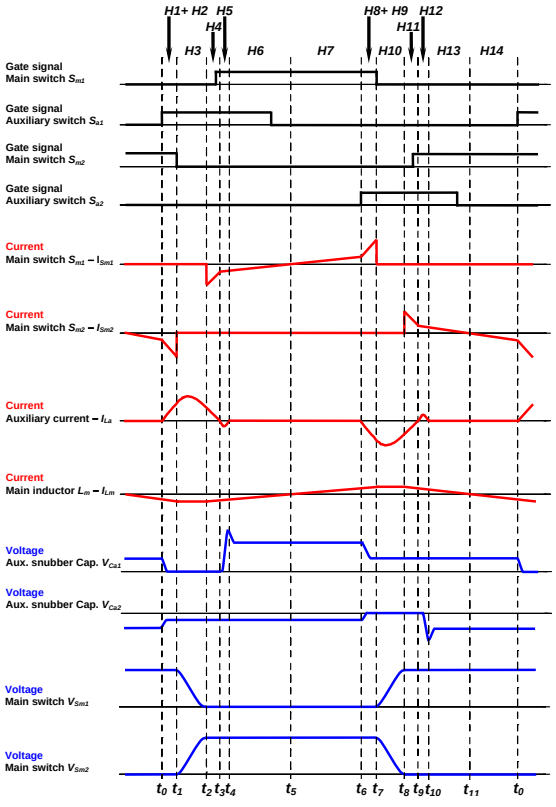
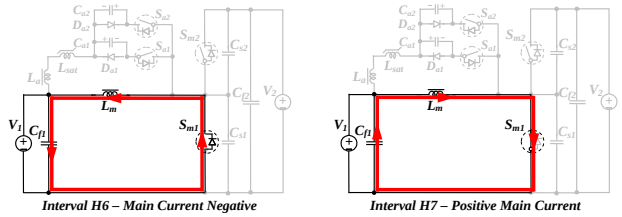
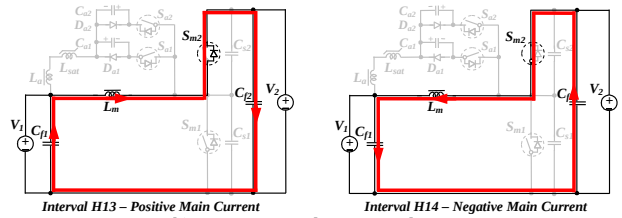


Figure 6. Basic waveforms in hybrid mode



a) Main current increasing $dI > 0$



b) Main current decreasing $dI < 0$

Figure 7. Main circuit intervals in hybrid mode

inductor is steadily decreasing from its maximum value. The current change rate dI is defined as $(V_1 - V_2)/L_m$. In the time instant t_{11}, the current seamlessly crosses though zero and Interval H14 starts. The state of converter switches remains unchanged during this transition. The intervals differ only in the reversed direction of the main inductor current. Interval H14 ends by turning *on* the switch S_{a1} and the next switching cycle begins by initiating the boost auxiliary pulse.

C. *Boost and Buck Auxiliary Current Pulses*

Boost and Buck auxiliary current pulses are formed during seven time intervals. Some intervals are missing in hybrid operation since extended reverse conduction (ERC) is always required due to low values of the main current. Therefore the reverse recovery of the main diode can be neglected. Since the method used to form and control these two pulses is the same, both pulses are discussed together in the following paragraphs. The discussion refers to circuit arrangements shown in Figure 8 in all cases where directions of current flow and converter state should be observed for better understanding of these intervals.

1) ***Intervals F1, R1, H1, H8*** *– Damped Discharge of Auxiliary Snubber Capacitor (Figure 8a)*

The starting point of this interval is the turn-on of the auxiliary switch. Initially the auxiliary snubber capacitor may be charged to a certain voltage level depending on the operating point. If the capacitor is fully discharged during intervals F10/R10 then this interval is skipped. Otherwise, the capacitor is discharged in a resonant fashion and the auxiliary current commutates to the auxiliary diode. The rate of discharge is defined by the sum of the auxiliary inductance L_a and saturable inductance L_{sat} in its unsaturated state. The value of the snubber capacitor is in the order of a few *nF* and therefore the discharge is fast in spite of the large inductance (L_{sat} prior to saturation). At the beginning of this interval, the current through the auxiliary circuit is zero and therefore the auxiliary switch turns *on* with ZCS. As discussed above, the auxiliary diode turns on essentially with ZVS in all operating points due to the presence of the auxiliary snubber capacitor. The next interval begins when the auxiliary diode turns *on*.

In case of Hybrid Mode, the following intervals which concern main current commutation to the auxiliary circuit and reverse recovery of the main diodes are skipped. The reason for this is that the main current is too low to provide complete soft switching; the main and auxiliary current are added and therefore the main current does not commutate to the auxiliary circuit. In addition to that, ERC of SR (Interval H2/H9) is always used to attain the complete soft switching hence the main diode does not go through the recovery.

2) ***Interval F2, R2*** *– Main Current Commutation to Auxiliary Circuit (Figure 8b)*

The interval begins when the auxiliary capacitor is fully discharged and the auxiliary current starts flowing through the auxiliary diode. The main current I_{Lm} commutates from the main switch to the auxiliary circuit. The saturable inductor L_{sat} saturates a short while after the beginning of the interval. The rate of the current rise during this interval is limited by the auxiliary inductor L_a together with the residual inductance of the saturable inductor. This rate is defined by equation (1) in case of F2 and by equation (2) in case of R2.

$$di_{a1}/dt = (V_2 - V_1)/L_{a\_o} \quad (1)$$

$$di_{a2}/dt = V_1/L_{a\_i} \quad (2)$$

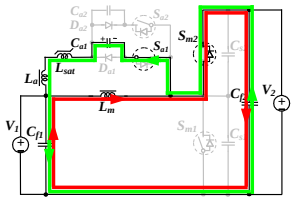
L_{a_o} is the total auxiliary inductance present in the auxiliary path between the input capacitor C_{f1} and output capacitor C_{f2} and L_{a_i} is the auxiliary inductance including connections to the input filter capacitor C_{f1}. The two values may slightly differ depending on the converter structural layout. The auxiliary current continues to rise until the moment it reaches the value of the main inductor current. In the same time, the current in the main switch reaches zero and the operation continues by the next time interval.

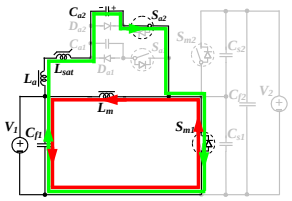
3) ***Interval F3, R3*** *– Reverse Recovery of Main Diode (Figure 8c)*

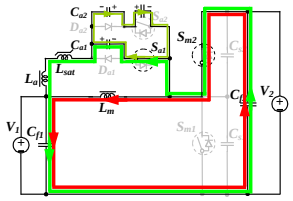
At the beginning of this interval, the main current has commutated fully to the auxiliary circuit and therefore the main diode must go through its reverse recovery. The recovery proceeds with the same *di/dt* as present in the previous interval. Selection of the auxiliary inductance L_a provides a degree of control over the *di/dt* and hence over the reverse recovery. If SR is used and ERC is not required for complete soft switching, the SR switch should be turned *off* at the zero current crossing to minimise the recovery. Once the recovery is over, the operation continues by Interval F5, R5. If ERC is required, the SR switch remains *on* beyond the zero current crossing and the circuit operation continues by the following time interval.

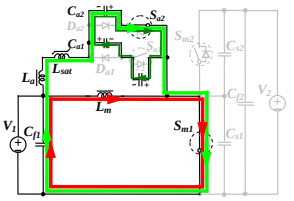
4) ***Interval F4, R4, H2, H9*** *– Building Up Current for Complete ZVS Turn-off of Main Switch (Figure 8d)*

This interval is used if the complete soft switching cannot be attained due to low load or small ratio between the input and output voltage. The auxiliary current continues rising with *di/dt* defined by (1) respectively (2). SR is turned *off*

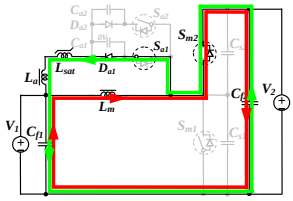


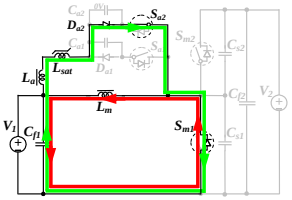




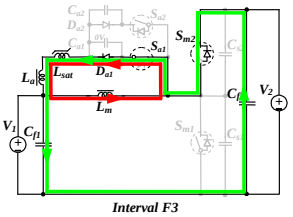


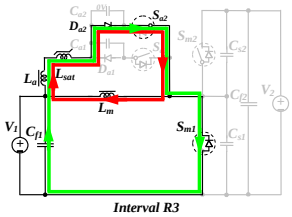
a) Damped discharge of auxiliary snubber capacitor



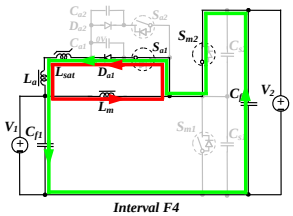


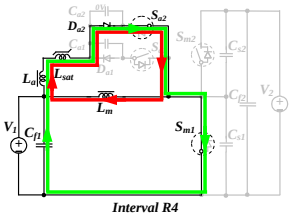
b) Main current commutation to auxiliary circuit

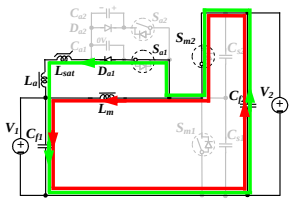


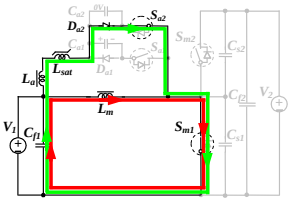


c) Reverse recovery of main diode

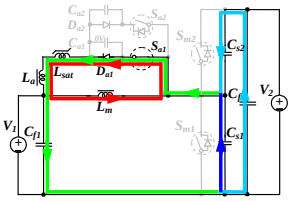


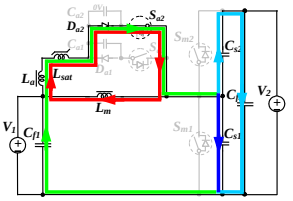


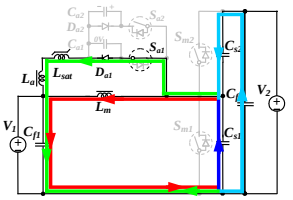


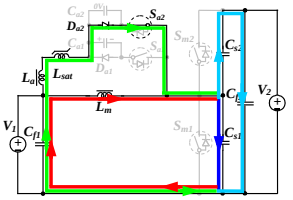


d) Building up current for complete ZVS turn *off* of main switch

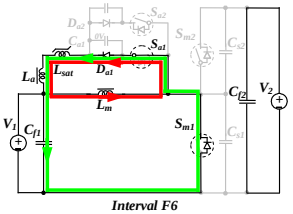


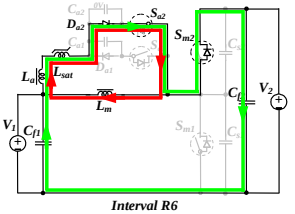


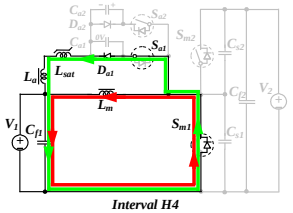


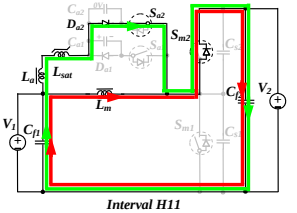


e) Resonant charge/discharge of main snubber capacitors

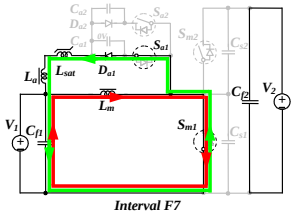


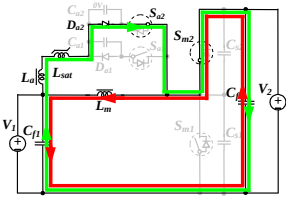




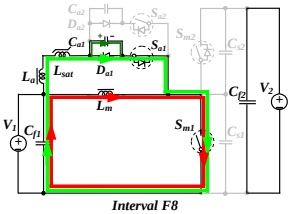


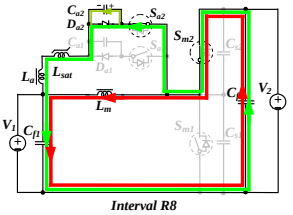
f) ZVS turn *on* of main switch

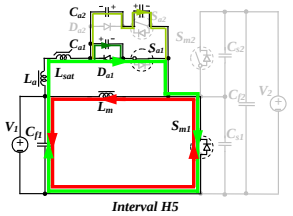


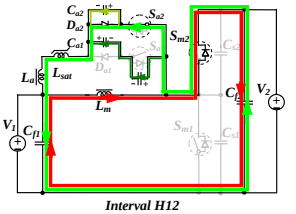


g) Main current commutation from auxiliary circuit to main switch









h) Reverse recovery of auxiliary diode

Figure 8. Operating modes involved in forming of auxiliary current pulse

when the auxiliary current reaches the value required for complete soft switching and the next interval begins.

5) ***Interval F5, R5, H3, H10*** *– Resonant Main Voltage Commutation (Figure 8e)*

At the beginning of this interval, the auxiliary current commutates to the snubber capacitors C_{s1} and C_{s2}. These can now be fully charged respectively discharged since the current has a required or higher than required value. The minimum auxiliary current required for complete resonant voltage transition and hence complete ZVS of main switches can be calculated by equation (3) for the boost pulse and by equation (4) for the buck auxiliary pulse.

$$I_{La\_\min} = V_2 \cdot \sqrt{\frac{C_{s1}+C_{s2}}{L_{a\_o}} \cdot \left(2\frac{V_1}{V_2} - 1\right)} \tag{3}$$

$$I_{La\_\min} = V_2 \cdot \sqrt{\frac{C_{s1}+C_{s2}}{L_{a\_o}} \cdot \left(1 - 2\frac{V_1}{V_2}\right)} \tag{4}$$

These equations apply for the output to input voltage ratio less than two in case of the boost and more than two in case of the buck pulse. In case of other voltage ratios, complete soft switching is possible even at zero current.

The charge and discharge processes can both be described by the following differential equations:

$$di_{aCs1}/dt = \left(V_1 - 1/C_{s1}\int i_{aCs1}\cdot dt\right)\Big/ L_{a\_i} \tag{5}$$

$$di_{aCs2}/dt = \left(V_2 - V_1 - 1/C_{s2}\int i_{aCs2}\cdot dt\right)\Big/ L_{a\_o} \tag{6}$$

$$V_2 = 1/C_{s1}\int i_{aCs1}dt + 1\Big/C_{s2}\int i_{aCs2}dt \tag{7}$$

The only difference between the two auxiliary pulses is in the initial conditions. The interval ends when the resonant transition is finished. In that instant, the auxiliary current commutates into the antiparallel diode of the main switch and the next interval begins.

6) ***Interval F6, R6, H4, H11*** *– ZVS Turn-on of Main Switch (Figure 8f)*

The current flow through the antiparallel diode of the main switch clamps the voltage across the switch to a near zero value, enabling ZVS turn-on. The main switch can be turned *on* with ZVS during the whole duration of this interval. The auxiliary current is reduced with *di/dt* calculated by equation (2) in case of the boost pulse respectively equation (1) in case of the buck pulse. The current reduction in the auxiliary circuit results in a current reduction in the antiparallel diode as well. When the current in the diode reaches zero, it commutates into the main switch and this time interval ends.

7) ***Interval F7, R7*** *– Main Current Commutation from Auxiliary Circuit to Main Switch (Figure 8g)*

During this interval, the main current slowly commutates from the auxiliary to the main switch. The commutation rate is identical to the previous interval. When the auxiliary current reaches zero and main switch carries the whole main current, the operation continues by reverse recovery of the auxiliary diode.

8) ***Interval F8, R8, H5, H12*** *– Reverse Recovery of Auxiliary Diode (Figure 8h)*

The reverse recovery of auxiliary diode is softened by the saturable inductance L_{sat} in its unsaturated state. When the recovery current stops, the rate of voltage rise across the diode is reduced by the auxiliary snubber capacitor and the overvoltage across the auxiliary diode is controlled. Depending on the circuit design, there may be a small overshoot due to the resonant character of the charge control circuit comprising of L_a, L_{sat} and the lack of clamping. The auxiliary switch may be turned *off* at any moment after the end of this interval and before turning *off* the main switch. In case of hybrid mode, the overlap of the two auxiliary switches should be avoided in order to prevent undesired circuit response. The turn-off is in all conditions under ZCS due to zero current flowing through the auxiliary switch when the turn-off command is given. In the same time, the auxiliary snubber capacitor provides ZVS conditions and therefore the turn-off is under ZCS combined with ZVS.

D. Timing of Auxiliary Pulses for Closed Loop Control

Closed loop control of soft switched converters is often considered difficult due to the necessity to precisely control numerous switches. The timing may be load dependant, which makes the matter even more complex. This is also the case for the proposed circuit where four switches must be timed precisely in order to attain complete soft switching in the whole operating region. Analytical equations for relevant timing are given below. The parameters required for these calculations include three measured values namely: input voltage V_1, output voltage V_2 and main inductor current I_{Lm} as well as circuit component parameters.

Detailed plots of the auxiliary current pulses are shown in Figure 9 and Figure 10. The analytical calculation must cover the time interval between t_0 and t_4 in order to execute the required timing. The auxiliary pulse starts by turning on the auxiliary switch. The turn-on is followed by a short non-linear region (from t_0 to t_{sat}) due to the presence of the saturable inductor. The intervals following after the saturation until t_2 are linear as described by equation (1) and (2) for boost and buck auxiliary pulse respectively. Since these equations are linear, the length of these intervals is fairly simple to evaluate. Following the linear intervals is the resonant charge/discharge of the snubber capacitors. Solving the resonant circuits shown in Figure 11 requires solving system of differential equations (5) to (7) with appropriate initial conditions for the two auxiliary pulses. The solution describing the resonant current through the auxiliary inductance L_a in the case of the boost pulse is:

$$i_{La}(t) = I_{ini\_F}\cdot\cos\omega_0 t + \frac{dV}{L_a\omega_0}\sin\omega_0 t \tag{8}$$

where I_{ini_F} is the initial current at the beginning of the resonant interval, dV is the difference between the output and input voltage calculated as $dV=V_2-V_1$, L_a is the auxiliary inductance value and ω_0 is the angular resonant frequency calculated as follows:

$$\omega_0 = 1/\sqrt{(C_{s1}+C_{s2})\cdot L_a} \quad (9)$$

The voltage of the snubber capacitor C_{s1} can be described by the following equation:

$$v_{Cs1}(t) = -\frac{I_{ini\_F}}{(C_{s1}+C_{s2})\cdot\omega_0}\cdot\sin\omega_0 t + dV(\cos\omega_0 t - 1) \quad (10)$$

Duration of the resonant interval (t_3–t_2) can then be found by solving equation (10) for v_{Cs1} equal to V_2 which yields:

$$t_3 - t_2 = \frac{2}{\omega_0}\cdot\arctan\left(-K + \sqrt{K^2 + \frac{dV+V_1}{dV-V_1}}\right) \quad (11)$$

where K is expressed as:

$$K = \frac{I_{ini}}{2\omega_0 C_s (dV - V_1)} \quad (12)$$

and I_{ini} is the initial current in this case equal to I_{ini_F}. Main switch S_{m1} can turn-on at any moment after t_3 and before t_4.

In case of the buck pulse, solving (5) to (7) results in the following equation describing the voltage of the C_{s2} capacitor:

$$v_{Cs2}(t) = \frac{I_{ini\_R}}{(C_{s1}+C_{s2})\cdot\omega_0}\cdot\sin\omega_0 t - V_1(\cos\omega_0 t - 1) \quad (13)$$

Duration of the resonant charge/discharge is then found by solving $v_{Cs2}(t) = V_2$ and the result is:

$$t_3 - t_2 = \frac{2}{\omega_0}\cdot\arctan\left(K - \sqrt{K^2 - \frac{dV+V_1}{dV-V_1}}\right) \quad (14)$$

where K is defined by equation (12) using the initial current I_{ini}=I_{ini_R}. The main switch S_{m2} may be turned *on* at any moment after t_3 and before t_4.

Complete soft switching requires that the part below the square root in equations (11) and (14) is positive. If this is not fulfilled, the resonant charge/discharge is not complete and the converter operates in partial hard switching mode. The soft switching boundary is derived by solving equation (15) in the case of the boost and equation (16) in the case of the buck auxiliary pulse.

$$K^2 + \frac{dV+V_1}{dV-V_1} = 0 \quad (15)$$

$$K^2 - \frac{dV+V_1}{dV-V_1} = 0 \quad (16)$$

Manipulating equations (15) and (16) results in equations (3) and (4) respectively. These equations are depicted in their graphical form in Figure 12. As shown, for $V_2/V_1 > 2$ in case of the boost pulse and for $V_2/V_1 < 2$ in case of the buck pulse, complete charge / discharge of snubber capacitors can be achieved even at zero initial current. For all other cases, a minimal current is required for complete soft switching. The overlap between the SR and the auxiliary switch (interval t_0 – t_2) should be controlled in such a way that this minimal current is always attained. The procedure for adjusting the overlap is discussed in the following paragraph.

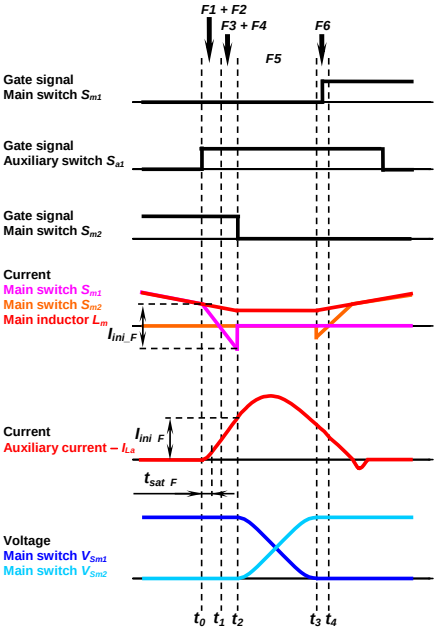


Figure 9. Detailed view of boost auxiliary pulse

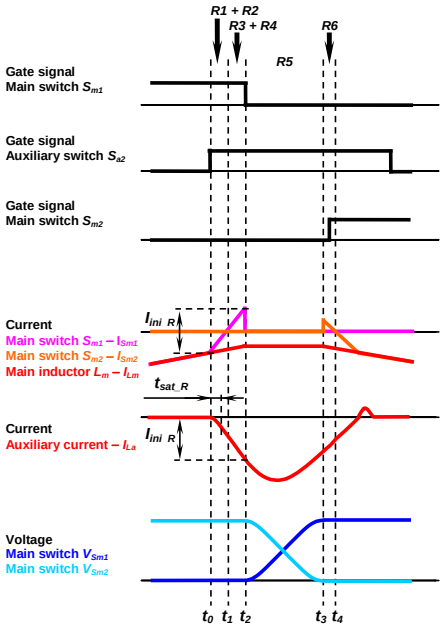


Figure 10. Detailed view of buck auxiliary pulse

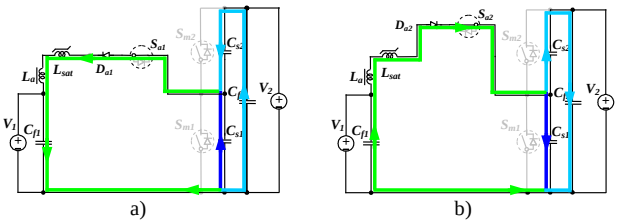


Figure 11. Resonant charge/discharge of snubber capacitors, a) boost auxiliary pulse, b) buck auxiliary pulse

E. Optimal Control of Extended Reverse Conduction (ERC) of SR Switch

Optimal control of ERC of SR switch aims to reduce switching losses in main switches by complete soft switching. This means that the initial current for resonant intervals F5, R5, H3 and H11 should always equal to the minimal value required for the complete soft switching. Needless increase of this current results in a higher auxiliary current than necessary which in turn results in higher auxiliary losses and hence reduced efficiency.

Required extension of reverse conduction is directly related to the main inductor current I_{Lm} and more specifically to so called minimums of this current associated with forward boost $I_{Lm\_min\_F}$ and reverse buck mode $I_{Lm\_min\_R}$ calculated as:

$$I_{Lm\_\min\_F} = I_{Lm} - dI/2 \quad (17)$$

$$I_{Lm\_\min\_R} = I_{Lm} + dI/2 \quad (18)$$

dI is the current ripple calculated as follows:

$$dI = \frac{V_1 \cdot t_{on\_S_{m1}}}{L_m} \quad (19)$$

where t_{on_Sm1} is the *on* time of S_{m1} switch.

At this point the reverse recovery of the main diode (diode of S_{m2} in forward boost operation and diode of S_{m1} in reverse buck operation) must be addressed since it contributes to auxiliary current build-up and hence it assists in attaining the soft switching. The recovery must be considered even if SR is employed since SR aids in reducing the recovery current but this current cannot be reduced below a minimum value I_{rr_min}. This value is highly design and component-dependent. The simplest method of its identification is experimental measurement with SR timed to minimise the reverse recovery.

First step in assessing the need for ERC is comparing the respective I_{Lm_min} currents to the minimum current value required to attain the complete soft switching. The ERC is needed if respective minimum current fulfils the following:

$$-I_{0\_F} < I_{Lm\_\min\_F} < I_{0\_F} - I_{rr\_\min} \quad (20)$$

$$-I_{0\_R} + I_{rr\_\min} < I_{Lm\_\min\_R} < I_{0\_R} \quad (21)$$

Figure 13 depicts the main current waveform for a general boost and buck case. Relevant current values and boundary conditions are marked in the figure. Red regions represent equations (20) and (21). If any of the two I_{Lm_min} values falls into the red region then ERC is required. Please note that I_{0_F} and I_{0_R} are not identical and that they vary with input and output voltage as depicted in Figure 12. If any of the two values is zero (boost pulse $V_2 > 2V_1$, buck pulse $V_2 < 2V_1$), then the particular red region vanishes and the extended conduction is not required.

The current build-up by ERC is controlled by the overlap between the relevant auxiliary and main switch as indicated in Figure 9 and Figure 10. The overlap can be calculated as:

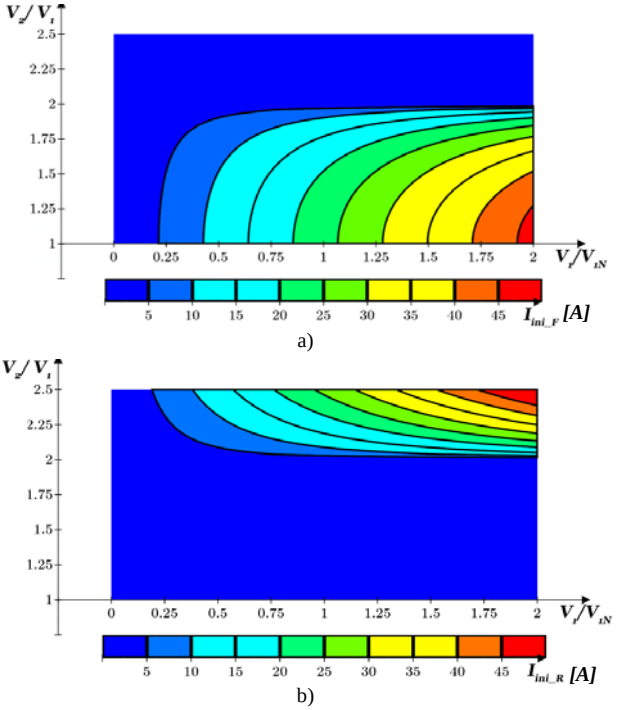


Figure 12. Minimal initial current required for complete soft switching and its dependence on input and output voltage in case of a) boost auxiliary pulse, b) buck auxiliary pulse; normalised to input voltage $V_{1N} = 200$ V

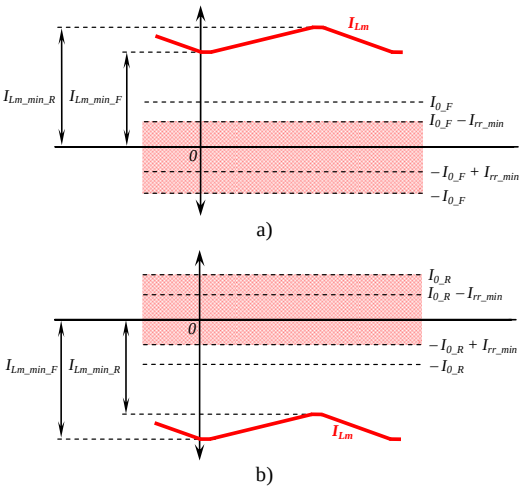


Figure 13. Main inductor current a) in boost mode b) in buck mode and with marking relevant value for assessing extended conduction of SR switch

$$I_{Lm\_\min\_F} > 0$$

$$t_2 - t_0 = L_a\left(I_{0\_F} - I_{rr\_\min} - I_{Lm\_\min\_F}\right)/dV \quad (22)$$

$$I_{Lm\_\min\_F} \le 0$$

$$t_2 - t_0 = L_a\left(I_{0\_F} - I_{Lm\_\min\_F}\right)/dV \quad (23)$$

$$I_{Lm\_\min\_R} < 0$$

$$t_2 - t_0 = L_a\left(I_{0\_F} - I_{rr\_\min} - I_{Lm\_\min\_F}\right)/V_1 \quad (24)$$

$$I_{Lm\_\min\_R} \ge 0$$

$$t_2 - t_0 = L_a\left(I_{0\_R} - I_{Lm\_\min\_R}\right)/V_1 \quad (25)$$

When the respective I_{Lm_min} crosses through the zero axis ($I_{Lm\_min\_F} \leq 0$, $I_{Lm\_min\_R} \geq 0$), the SR switch is expected to assume the full control of the current turn-off process, the reverse recovery does not occur and therefore I_{rr_min} is eliminated in equations (23) and (25).

F. Control of Auxiliary Switches in Hybrid Mode

The main difference between the hybrid mode and boost respectively buck mode is that both auxiliary switches are active. Using both auxiliary switches results in additional losses due to double auxiliary current pulse and therefore it should be avoided at higher currents when it is not necessary.

The enable function of the auxiliary switches is controlled in hysteresis manner as illustrated in Figure 14. The measured main inductor current is compared to the four boundary values as indicated. The auxiliary switch S_{a2} is enabled at $I_{H\_EN\_F}$ and disabled at I_{F_EN} where as S_{a1} is enabled at $I_{H\_EN\_R}$ and disabled at I_{R_EN}. The gap between the I_{F_EN} and $I_{H\_EN\_F}$ respectively I_{R_EN} and $I_{H\_EN\_R}$ is set such that oscillations between the single auxiliary pulse modes and the hybrid mode due to noise in the current measurements or slight load variations are prevented.

III. Converter Prototype

In order to verify the operation of the proposed circuit, a converter prototype was built and tested. The prototype specifications target applications in drive trains of electric, hybrid and fuel cell vehicles. Main design parameters are listed in Table II. The circuit diagram of the converter prototype is shown in Figure 15 whereas the relevant component values and types are listed in Table III. Using R_{DSon} optimised Super-Junction MOSFETs means that poor dynamic performance of their body diodes [15] must be addressed in the converter design. The advantage of the proposed topology is that it can effectively control reverse recovery of the body diode as discussed above. The issue of forward recovery is in the presented design dealt with by using fast Si diodes ($D_{p1\_1} - D_{p2\_2}$ in Figure 15) in parallel to main MOSFETs. These diodes are much faster than the body diodes of the used SJ MOSFETs and therefore they can handle very fast current commutations from snubber capacitors as present in intervals F11, R11, H4 and H11. Detailed discussion on dealing with poor dynamic performance of SJ MOSFET body diodes in the proposed topology is published in [16]. IGBTs are used as the auxiliary switches. The reason for this is that they are better suited to the pulse-like auxiliary current since they exhibit much lower voltage drops than MOSFETs at high current values. The trade-off was made in order to reduce the conduction losses in the auxiliary circuit close to full power output.

Two SJ MOSFETs are used in parallel in order to reduce the conduction losses and to improve SR. Switching performance of paralleled SJ MOSFETs under hard as well as soft switching was tested in [15]. These devices perform well under such conditions if gate resistances are balanced. However, the use of parallel devices may result in current

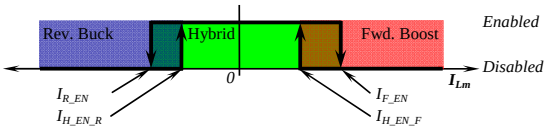


Figure 14. Hysteresis control of Hybrid mode operation

TABLE II Main Design Parameters

Nominal input voltage V_{1N}	200 V
Nominal output voltage V_{2N}	400 V
Maximum input current I_{1M}	70 A
Nominal output power P_{2N}	14 kW
Operating frequency f_s	62.5 kHz

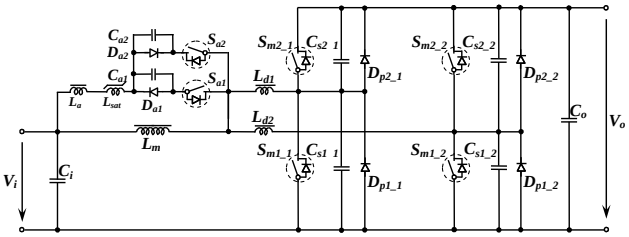


Figure 15. Circuit diagram of converter prototype

TABLE III. Design Values and Types of Main Components

Main inductor L_m	50 µH
Aux. inductor L_a	1.2 µH
Sat. inductor L_{sat}	4 x W914 [18]
Decoupling inductors L_{d1}, L_{d2}	320 nH
Snubber capacitors C_{s1_1}, , C_{s1_2}, C_{s2_1}, C_{s2_2}	2 x 3.6 nF
Aux. snubber capacitors C_{a1}, C_{a2}	0.9 nF
Main switch S_{m1}, S_{m2}	2 x STY112N65M5 [19]
Parallel diodes D_p	DSEE29-12CC [20]
Aux. switch S_{a1}, S_{a2}	IRG4PSC71UD [21]
Aux. diodes D_{a1}, D_{a2}	DSEE29-12CC [20]
DSP controller	TMS320F28335 [22]

oscillations between the two switches due to stray inductance of relevant connections. In order to prevent this, decoupling inductors L_{d1}, L_{d2} are used to dampen the oscillations. Even a small value such as 320 nH is very effective. It should be noted that the decoupling inductors must be accounted for in the auxiliary circuit design (included in L_a value) since they are in the auxiliary current path.

The original topology proposed in [10] performed well considering the conversion efficiency but it suffered from voltage spikes across the auxiliary diodes. The spikes are cause by the auxiliary diode reverse recovery suddenly interrupting the auxiliary current. Energy stored in the auxiliary inductor L_a causes the overvoltage as shown in Figure 16a. The overvoltage can be high in spite of the small value of the auxiliary inductance and the small current being interrupted. In the modified topology proposed in this paper, this is prevented by auxiliary snubber capacitors and saturable inductor in the auxiliary current path.

The impact of saturable inductor and auxiliary snubber capacitors on the overvoltage and consecutive ringing is demonstrated by waveforms shown in Figure 16. As shown, the saturable inductor is very effective in suppressing the overvoltage. However, the overvoltage is fully under control

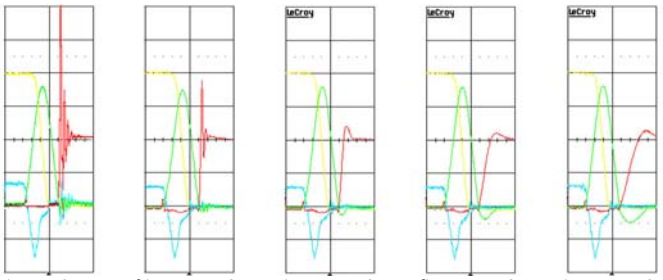
only when the inductor is combined with the snubber capacitors. The "optimal" values of the snubber capacitors and the saturable inductor were found experimentally, as the non-linear nature of saturable inductor makes analytical approach rather complex. The optimisation process is demonstrated by waveforms shown in Figure 16. As shown, the capacitance value of 0.9 nF combined with four W914 nanocrystalline ring cores [18] results in the voltage spike being reduced to as little as 120 %. In the same time, the spike is very smooth. Further capacitance and inductance increase suppresses and smoothes the spike even more but the efficiency is reduced.

It should be obvious from Figure 16 that the voltage spike was largely suppressed while the efficiency was reduced by approximately 1 %. Since the tests were performed at the output power of 1 kW, the reduction is much smaller at higher power levels (compared to experimental results on the circuit shown in Figure 1 published in [10], the efficiency reduction at 12 kW, 200 V to 400 V conversion is approx. 0.2 %). A similar voltage spike reduction could be attained by using a larger saturable inductor only. However, the impact on the efficiency would be much larger since a larger core would be saturating in every switching period. It may seem that the snubber capacitors make the snubber much more complex than the original circuit shown in Figure 1. However, in reality the 0.9 nF capacitors are high voltage ceramic chips soldered directly to diode leads and therefore impact on the converter structure complexity is nonexistent. The implementation of saturable inductor is very simple as well. The inductor is made of four beads 8 mm in diameter threaded on the connecting cable leading to the auxiliary inductor L_a. It must be noted however that cooling the rings is important in the final prototype since in the hybrid mode they saturate twice per switching period and the related loss must be effectively removed.

A. Experimental Results

All experimental tests described in this paragraph were performed under closed loop operation with output voltage control. The timing algorithms as discussed above as well as the current and voltage controller were implemented in a single TMS320F28335 DSP. The same DSP was also used to generate the control pulses for individual switches. A new set of control parameters was loaded into the PWM unit every eighth switching period (128 µs control period). The calculation of the control commands as well as of the switch timing occupied approximately 25 % of the available time slot. The controllers were tuned to accept a step load change as well as an output voltage step change. They performed well under all testing conditions.

Input as well as output voltages and currents were measured by a digital power meter with precision current sensors. Resulting efficiency and loss curves are plotted in Figure 17 and Figure 18 respectively. The measurements were performed in a wide load range and various input to output conversion ratios. The peak efficiency is reached at 50 % of the input current for all voltage ratios and both directions of operation. The peak efficiency value is close to 98.5 % for the 1.25 voltage ratio. The peak is reduced to 98.2 % at the voltage ratio equal to 2. Reducing the voltage ratio to 1.1 in buck operating mode resulted in reduced efficiency due to a high auxiliary current required to maintain complete soft switching. In all other tested cases, the losses in buck and boost operation are almost equal and the efficiency curves are symmetrical. Notice a small hump, in the loss curves in the zero power region. This hump represents converter operating in the hybrid mode. The losses in this region are slightly higher than in the pure buck and boost regions because of the two auxiliary current pulses. The two pulses mean double the conduction losses in the auxiliary circuit. The loss increase due to the second pulse is estimated at 10 W and therefore it can be considered negligible from the thermal point of view.



a) L_{sat} = 0 H, C_a = 0 F, η = 96.7 %
b) L_{sat}=4xW914, C_a = 0 F, η = 95.5 %
c) L_{sat}=4xW914, C_a = 0.9 nF, η = 95.7 %
d) L_{sat}=4xW914, C_a = 3.6 nF, η = 95.2 %
e) L_{sat}=4xW914, C_a = 8.3 nF, η = 94.4 %

Figure 16. Voltage ringing across auxiliary diode at various circuit configurations, V_i = 200 V, V_o = 400 V, P_o = 1 kW; CH1 – Yellow – V_{DS} of S_{m1} switch – 100 V/div, CH2 – Red – V_{AK} of D_{a1} diode – 100 V/div, CH3 – Cyan – I_D of S_{m2} switch – 5 A/div, CH4 – Green – I_{Lsat} – 10 A/div, time scale 1 µs/div

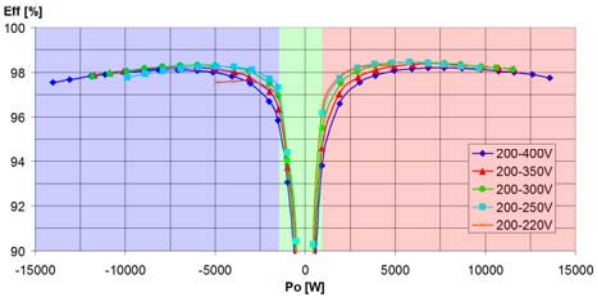


Figure 17. Measured efficiency curves; Boost mode – red, Buck mode – blue, Hybrid mode – green

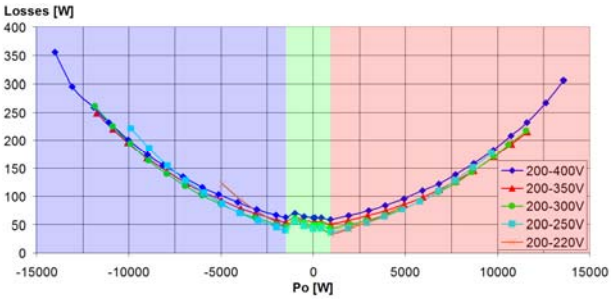
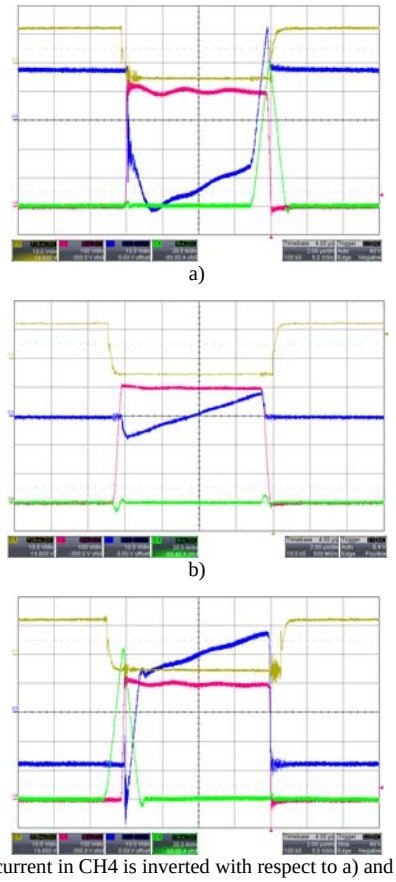


Figure 18. Power loss vs. output power; Boost mode – red, Buck mode – blue, Hybrid mode – green



a)

b)

c) (current in CH4 is inverted with respect to a) and b))

Figure 19. Measured waveforms at a) maximum negative current (buck mode), b) zero current (hybrid mode) c) maximum positive current (boost mode); CH1 – Yellow – V_{GS} of S_{m1} switch – 10 V/div, CH2 – Magenta – V_{DS} of S_{m1} switch – 100 V/div, CH3 – Blue – I_D of S_{m2} switch – 10 A/div, measured by Rogowski current probe - zero current does not match indicated position, CH4 – Green – I_{Lsat} – 20 A/div, time scale 2 µs/div

Waveforms measured at maximum negative current (buck operation), zero current (hybrid operation) and maximum positive current (boost operation) at 200 V to 400 V conversion (voltage ratio of 2) are shown in Figure 19 a–c. The scale is identical for all the figures. Notice the two auxiliary current pulses at zero output current. As shown, irrespective of the operating point, all converter waveforms are noise and oscillation-free due to complete soft switching. Similar behaviour was also observed at other output to input voltage ratios.

IV. Conclusions

The paper discusses a dc-dc converter topology with complete soft switching in the whole operating region. It is based on auxiliary resonant commutated pole (ARCP) applied to dc-dc buck/boost topology. The basic operation was improved and the proposed circuit achieves complete soft switching, low stress and noiseless waveforms for all the components.

Analytical equations were derived for closed loop control of the proposed circuit. These were implemented in the controller of the experimental prototype. The prototype was tested in the whole power range from –14 kW to +14 kW with efficiency over 98 % in a wide load range. Complete soft switching at zero load and essentially noiseless operation in all operating points were demonstrated as well.

One of the main motivations behind the proposed topology was also to keep it as simple as possible. The simplicity was especially important from the ease of structural layout point of view. The proposed circuit is arranged in such a way that most of the critical connections between the submodules are not sensitive to stray inductance of interconnects. A few connections that are critical involve only simple parallel connections between two components and therefore they can be made as short as possible. A high power density converter design may also benefit from the layout simplicity. Power density over 50 kW/l can be expected if optimal structural and thermal design are used.

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