Partial Power Conversion Device Without Large Electrolytic Capacitors for Power Flow Control and Voltage Compensation

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***Abstract*—A novel partial power conversion device (PPCD) is proposed to realize power flow control and voltage compensation in a three-phase power distribution system in this paper. The PPCD circuit, which is derived from the conventional push–pull forward converter, can achieve arbitrary voltage output without any large electrolytic capacitors. Thus, the system reliability can be enhanced. Furthermore, the converter has no full-rated components, which reduces the cost. In this paper, an injection model for power flow control is derived. A minimum power transfer control strategy is proposed to minimize the power losses during the operation. A closed-loop control method employing the synchronous reference frame theory for voltage compensation is also developed to enable the precise control. The systems with PPCD are simulated by MATLAB/Simulink to verify the functions. The experiments for voltage compensation are carried out based on a 30-kW prototype, which shows the effectiveness.**

***Index Terms*—Flexible ac-transmission system (FACTS) device, inverterless converter, partial power conversion, power flow control, voltage compensation.**

I. Introduction

As the price of the fossil fuel keeps on growing in the last decades, the government and public people show great interest to the renewable energy applications. The fossil-fuel-based generation system is shifting to the renewable energy-based generation one in the electric grid, which is promoted by the government in many countries [1]. The increasing penetration of renewable energy, the growing demand of the electrical power, and the aging of networks make it desirable to control the power flow in power-transmission systems fast and reliably [2]. On the other hand, as the rapid development of the industrial economy, soaring installation of the nonlinear loads greatly degrade the power quality of the grid. Reactive power variations and voltage fault such as voltage harmonics, voltage sag, and voltage surge occur occasionally, which increases the transmission losses and cause the nearby sensitive equipment to malfunction [3]. In order to meet the power quality requirement defined in the IEEE 519 [4] to avoid the large penalties and protect the nearby equipment, additional compensation devices installation is inevitable.

Traditional offline optimal power flow control techniques, including setting the operating points of various generators, shunt VAR compensation, and load tap-changing setting, may not be the desirable solutions mainly because of the large reactive loop current which may cause in a meshed grid structure and also the slow response time due to the complex algorithm [1].

The unified power flow controller (UPFC), which is considered as the most powerful flexible ac-transmission system (FACTS) device [5], can be utilized to control the power flow in power-transmission system [6], [7]. The same structure applied in power-distribution system, which is named as unified power quality conditioner (UPQC), is designed to perform the compensation functions for voltage sag/swell, voltage harmonics, and reactive power [8]. The UPFC device has two inverter-type converters coupled with a common dc link [5]. The series inverter injects a four-quadrant voltage with controllable magnitude and phase in series with the line to realize multiple functions such as power flow control and voltage compensation at the same time. However, the UPFC device needs a large energy storage element in the dc-link part, which is usually the electrolytic capacitor with short lifetime [9]. As a result, it has problems when installed to the power system with high reliability requirements. In order to overcome the drawbacks, an improved device named distributed power-flow controller (DPFC) [5] is proposed based on the new distributed FACTS concept [10]. The DPFC device, which has the same function as the UPFC, eliminates the common dc link between the shunt and series inverters. It has lower cost and higher reliability than the UPFC devices. Nonetheless, the DPFC device still has the large capacitors installed in both its shunt and series inverter, which means that the reliable issue has not been essentially solved. In the microgrid system, distributed structures based on the UPQC devices are discussed in [11]–[13]. The concept of these scenarios is to make use of the existing inverters which are connected to renewable energy sources or energy storage devices to implement the aforementioned functions. However, the applicable areas of these scenarios are apparently limited in the grid that has plenty of distributed generation devices. Thus, these solutions are hard to extend to most of the applications.

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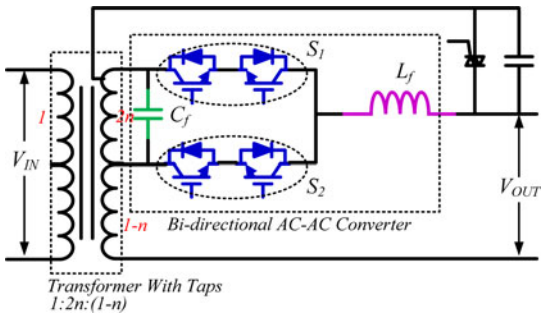

Fig. 1. Basic circuit of a CNT [1], [2], [19], [21], [22].

The large energy storage elements can be eliminated by employing the direct ac–ac conversion technology, such as the ac–ac choppers [14] or the matrix converters [15]. Several compensators are proposed based on these topologies [16]–[18]. However, among these solutions, either too many switches or a full-rated conversion part is necessary, which increases the cost. Besides, the control strategy of these converters are always complex, which lead to low reliability and difficult fault ride-through handling.

Recently, a new concept in the direct ac–ac power conversion field is proposed [1], [2], [4], [9], [19]–[23]. It applies the dual virtual quadrature sources (DVQS) voltage synthesis theory to the traditional ac–ac choppers to achieve the required voltage output. Its parallel form is implemented to power factor correction and current harmonic filtering [4], [20]. Its series form shown in Fig. 1 [1], [2], [19], [21], [22], which is named as the controlled network transformer (CNT), is realized by augmenting an existing load-tapping transformer with a fractionally rated bidirectional ac–ac converter. It is proposed to control the power flow in the meshed grid system by controlling the amplitude and the phase of the output voltage. According to the simulation results [1], [2], [19], by applying the CNT, the power system transfer capacity can be increased without additional wires. At the same time, the system dynamic is also enhanced. Compared with the former developed technology, the CNT has higher reliability, lower power rate, and lower cost [19]. However, the CNT still consists of a full-rated transformer, which is costliness. In addition, the aforementioned papers have not discussed about dealing with the power quality issues, which is also important for modern electric grid.

In this paper, a novel partial power conversion device (PPCD) is proposed to realize power flow control and voltage compensation in the three-phase power distribution system. The PPCD circuit can achieve arbitrary voltage output without any large electrolytic capacitors. Thus, the system reliability can be enhanced. Furthermore, the converter has no full-rated components, which reduces the cost. In this paper, the injection model for power flow control is derived. A minimum power transfer control strategy is proposed to minimize the power loss during the operation. A closed-loop control method employing the synchronous reference frame (SRF) theory for voltage compensation is also developed to enable the precise control. This paper is organized as follows. The basic block of the PPCD is demonstrated and analyzed in Section II. The model for power flow control is derived in Section III with the control range given and a minimum power transfer control strategy is proposed. The system configuration and closed-loop control method for voltage compensation is derived in Section IV. The simulation and experimental results are displayed and analyzed in Section V, which shows the effectiveness of the proposed PPCD. The last section summarizes the conclusions drawn from the investigation.

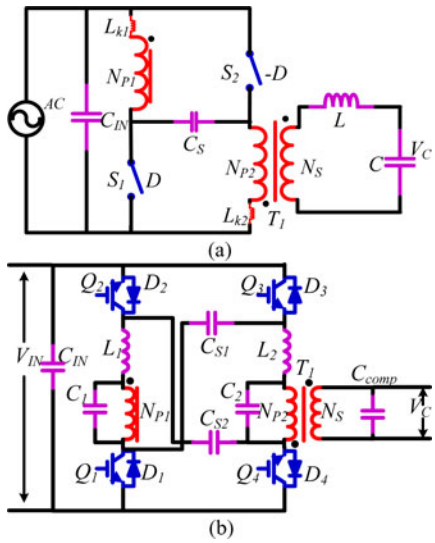

Fig. 2. Evolution of a PPCD circuit. (a) Original ac–ac push–pull forward converter. (b) Final version of a PPCD circuit.

II. PPCD Circuit Demonstration and Analysis

The proposed PPCD circuit is derived from the push–pull forward dc-dc converter [24]. Fig. 2(a) shows the schematic of the ac–ac push–pull forward converter where the input and output voltage is ac and the MOSFET S_1 and S_2 are replaced by two bidirectional switches. The transformer T_1 is a three-winding transformer where the turns of two primary side and secondary side are n_{P1}, n_{P2}, and n_s, respectively. The turn ratio N of T_1 is expressed as $N = n_s/n_p$ where $n_P = n_{P1} = n_{P2}$. The coupling reference is pointed by "$*$." The advantage of the topology is that the energy in the leakage inductances L_{k1} and L_{k2} of T_1 can be absorbed and recycled by adding a clamping capacitor C_S. As a result, the voltage stress on S_1 and S_2 is limited.

The final version of the PPCD circuit is derived by reforming the ac–ac push–pull forward topology circuit. As shown in Fig. 2(b), each bidirectional switch in Fig. 2(a) is realized by two separated IGBTs with antiparallel diodes. Thus, the connected IGBTs Q_2-Q_3 and Q_1-Q_4 can be replaced by the IGBT bridge-type module, respectively, which facilitates the high power application for this circuit. As a trade-off, two clamping capacitors C_{s1} and C_{s2} are required as shown in Fig. 2(b). In the final version, the output LC filter is moved from the secondary side of the transformer N_S to both primary sides N_{P1} and N_{P2}. As a result, the high-frequency harmonic components superposed on

TABLE I
SELECTION OF SWITCHING PATTERNS ACCORDING TO INPUT VOLTAGE

mode	Input Voltage	Q_1	Q_2	Q_3	Q_4
(a)	"+"	High frequency switching	Normal on	High frequency switching	Normal on
(b)	"-"	Normal on	High frequency switching	Normal on	High frequency switching

N_{P1} and N_{P2} are eliminated. The transformer, thus, is easier to design.

Pulsewidth modulation technique is implemented to generate the switching signals for the IGBT Q_1-Q_4. The generation of the switching patterns depends on the different polarities of the input voltage, which is shown in Table I. When the input voltage $V_{\rm in}$ is positive during the operation, Q_1 and Q_3 are switched in high frequency, whereas Q_2 and Q_4 are normally ON. The gate signals of Q_1 and Q_3 in this case are complementary with additional enough dead time. The switching patterns are reversed when $V_{\rm in}$ is negative, which are also given in Table I.

The two circuits in Fig. 2 have the same voltage transfer characteristic which can be attributed to buck-type essentially. So the voltage gain analysis can be based on the circuit displayed in Fig. 2(a). The duty ratio of the bidirectional switch S_1 is defined as D. The duty ratio of S_2 is defined as $-D$. The control range of D is $[-1, 1]$ where "-1" means normal OFF and "1" means normal ON. The turn ratio N of T_1 is expressed as $N = n_s/n_p$ where $n_P = n_{P1} = n_{P2}$. The output voltage V_C of the circuit can be derived by applying the principle of inductor volt–second balance and using the small-ripple approximation; the result is displayed as follows:

$$V_C = V_{\rm in} \cdot D \cdot N. \tag{1}$$

Assuming that the circuit is lossless, the input current is $I_{\rm CON}$ and the output current is I_C; the power rate of the ac–ac converter in the PPCD circuit is given as follows:

$$\begin{aligned} {\rm P_{rate}} &= \max\{V_{\rm in} I_{\rm CON}\} = \max\{V_C I_C\} = \max\{NDV_{\rm in} I_C\} \\ &= NV_{\rm in} I_C = NP_r. \end{aligned} \tag{2}$$

By defining the system power rate $P_r = V_{\rm in} \cdot I_C$, the result of (2) shows that the power rate of the converter is $N \cdot P_r$. Typically, N varies from 0.1 to 0.5, which means that the converter is a partial power converter. The conclusion is the same for the transformer T_1 since it transfers all the power go through the converter.

III. SYSTEM MODELING AND CONTROL METHOD ANALYSIS FOR POWER FLOW CONTROL

In this section, the system model with PPCD for power flow control is derived. Based on this model, the available control range is given and then a minimum power transfer control strategy is proposed to control the power flow at the same time to minimize the power loss of the converter.

Fig. 3 shows the typical system configurations with the proposed PPCD. The converter is placed between the generation area and the load area. The voltages of the two areas are separated by a phase difference δ. The original inductance of the transmission line is assumed to be L, where X_L represents its impedance. The PPCD injects a controllable compensation voltage V_C in series through the connection transformer T_1 to control the power flow. The PPCD then can be considered as a controllable voltage source. The input energy of PPCD is drawn from the generation area and the input current is $I_{\rm CON}$. According to (2), the power rate of the system is P_r and the power rate of the converter is $N \cdot P_r$. Compared with the solution in Fig. 1 [1], [2], [19], [21], [22], the ac–ac converters have the same partial rate $N \cdot P_r$ if the turn ratio N equals the tap ratio n in Fig. 1, while T_1 has the partial rate $N \cdot P_r$ compared to the full-rated transformer in Fig. 1. In order to make the analysis easier, the power loss of the transmission line and the PPCD is ignored in the analysis given in the following.

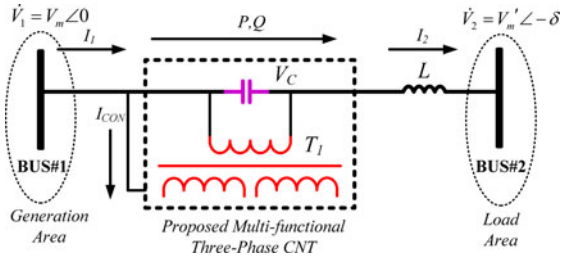

Fig. 3. Typical system configurations with the proposed PPCD for power flow control.

A. Power Flow Control Model Analysis

A well-developed model for the UPFC device is described in [25]. In this paper, the PPCD for power flow control is modeled similar with the modeling process mentioned in [25]. The system can be first modeled as Fig. 4(a) shows. The PPCD is represented by an ideal series voltage source V_C in series with the line impedance X_L. The voltage on BUS#1 and BUS#2 is given in (3) and (4), and the output voltage $V_{\rm OUT}$ satisfies (5)

$$\dot{V}_1 = \sqrt{2} V_m \sin \omega t \tag{3}$$

$$\dot{V}_2 = \sqrt{2} V_m' \sin(\omega t - \delta) \tag{4}$$

$$\dot{V}_{\rm OUT} = \dot{V}_1 + \dot{V}_C. \tag{5}$$

In order to generate an appropriate compensation voltage V_C to change the power flow between the two area, by applying the DVQS voltage synthesis theory and using the even harmonic modulation (EHM) scheme [9], the duty ratio D of the ac–ac converter is given in the form of a dc component K_0 added a second harmonic component where the amplitude and phase are K_2 *and* φ_2, respectively. It is expressed as follows:

$$D = K_0 + K_2 \sin(2\omega t + \varphi_2). \tag{6}$$

Substituting (3) and (6) into (1), the V_C can be calculated and given in complex form

$$\dot{V}_c = r\sqrt{2} V_m \angle \varphi \tag{7}$$

$$r = N\sqrt{\left(K_0 - \frac{1}{2}K_2 \sin\varphi_2\right)^2 + \left(\frac{1}{2}K_2 \cos\varphi_2\right)^2} \tag{8}$$

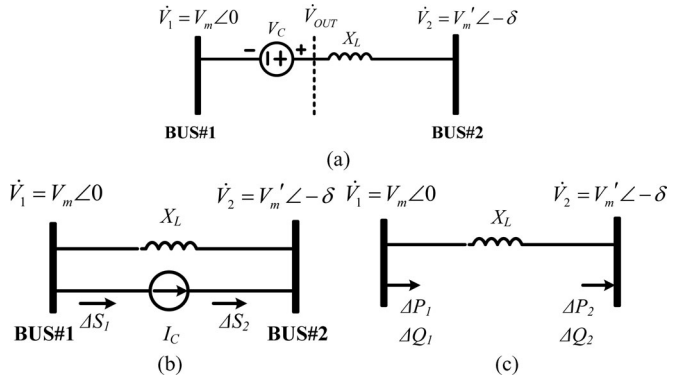

Fig. 4. Derivation of injection model for power flow control. (a) PPCD circuit being replaced by a voltage source. (b) Replacement of a voltage source by a current source. (c) Final injection model.

$$\varphi = \arctan\left(\frac{\frac{1}{2}K_2\cos\varphi_2}{K_0 - \frac{1}{2}K_2\sin\varphi_2}\right). \tag{9}$$

It should be noticed that because of the injection of second harmonic modulation signal, V_c consists of first and third components. In a symmetrical three-phase power system, the third harmonics can be naturally blocked and the expression for V_C is, thus, simplified.

In order to analysis the influence to the system after the compensation, an injection model for the system can be further obtained, which is shown in Fig. 4(b). The voltage source V_C is replaced by the current source I_c in parallel with the original line impedance X_L. The I_c satisfies the equation

$$\dot{I}_C = \frac{\dot{V}_C}{jX_L}. \tag{10}$$

The current sources I_C corresponds to the injection current after applying the power flow control, and the injection power ΔS_1 and ΔS_2 are expressed as

$$\Delta\dot{S}_1 = \dot{V}_1\cdot(\dot{I}_C)^* = \Delta\dot{P}_1 + \Delta\dot{Q}_1 \tag{11}$$

$$\Delta\dot{S}_2 = \dot{V}_2\cdot(\dot{I}_C)^* = \Delta\dot{P}_2 + \Delta\dot{Q}_2. \tag{12}$$

Further considering the effect of the converter current I_{CON}, the final model are demonstrated in Fig. 4(c). The injection power ΔS_1 is modified to

$$\Delta\dot{S}_1 = \dot{V}_1\cdot(\dot{I}_C)^* + \dot{V}_1\cdot(\dot{I}_{\mathrm{CON}})^* = \dot{V}_1\cdot(\dot{I}_C)^* + \dot{V}_c\cdot\left(\frac{\dot{V}_c+\dot{V}_2-\dot{V}_1}{jX_L}\right)^* = \Delta\dot{P}_1 + \Delta\dot{Q}_1. \tag{13}$$

The corresponding incremental active power flow ΔP_1, ΔP_2 and reactive power flow ΔQ_1, ΔQ_2 can be derived from (12) and (13); the results are given in (14)–(17). As soon as all the losses are neglected, ΔP_1 is equal to ΔP_2

$$\Delta P_2 = \frac{rV_m'V_m}{X_L}\sin(\delta+\varphi) \tag{14}$$

$$\Delta Q_2 = \frac{rV_m'V_m}{X_L}\cos(\delta+\varphi) \tag{15}$$

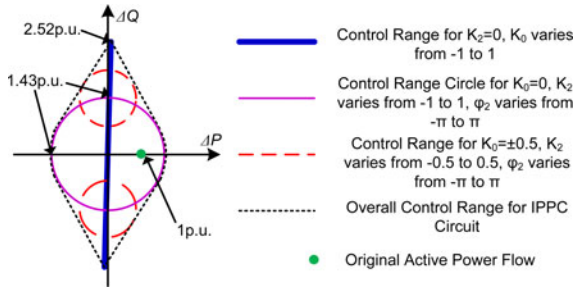

Fig. 5. Control range of a PPCD for power flow control.

$$\Delta P_1 = \frac{rV_m'V_m}{X_L}\sin(\delta+\varphi) \tag{16}$$

$$\Delta Q_1 = \mathrm{Im}\left\{\dot{V}_1\cdot(\dot{I}_C)^* + \dot{V}_c\cdot\left(\frac{\dot{V}_c+\dot{V}_2-\dot{V}_1}{jX_L}\right)^*\right\}. \tag{17}$$

The active power flow P_2 and reactive power flow Q_2 to the BUS#2 are the control targets. According to (14) and (15), the power flow control can be realized by changing parameters r and φ. Since r and φ are determined by dc value K_0, amplitude of the second harmonics K_2, and its phase φ_2 in duty ratio D, the power flow control can be realized by controlling the duty ratio D of its ac–ac converter with the installation of the PPCD.

B. Power Flow Control Range Derivation

As the duty ratio D has its range $[-1, 1]$, the parameters K_0 and K_2 are constrained by the following equation:

$$|K_0| + |K_2| \le 1. \tag{18}$$

The power flow control range of the PPCD can be derived by the analysis of (8), (9), (14), and (15). For example, in the original system without the PPCD, the active power and reactive power to BUS#2 is given by [10]

$$P_L = \frac{V_m'V_m}{X_L}\sin\delta \tag{19}$$

$$Q_L = \frac{V_m^2 - V_m'V_m\cos\delta}{X_L}. \tag{20}$$

Assuming that $\delta = 2^\circ$, $V_m \approx V_m'$. Then, it has $\sin\delta = 0.0349$, $\cos\delta = 0.9994$, $P_L \approx 1$ p.u., and $Q_L \approx 0$ p.u. The turn ratio N of the connection transformer is set to 0.1, which means that the power rate of the transformer is 0.1 p.u. Then, three typical conditions are analyzed in the following with the corresponding control range graph plotted in Fig. 5.

1) $K_2 = 0, K_0 \in [-1\ 1]$: Under this condition, (8) and (9) are simplified to $r = 0.1$ and $\varphi = 0$. By varying K_0, according to (14) and (15), it can be found that ΔP_2 will be always small but ΔQ_2 is changed a lot. This conclusion is true when δ is small enough, which is the normal condition for a transmission line. The maximum absolute values of ΔP_2 and ΔQ_2 are 0.10 p.u. and 2.52 p.u., respectively, when $K_0 = \pm 1$, which is shown in Fig. 5.

2) $K_0 = 0, K_2 \in [-1\ 1], \varphi_2 \in [-\pi\ \pi]$: Under this condition, (8) and (9) are simplified to $r = 0.05$ and $\varphi = \varphi_2$. Let $K_2 =$

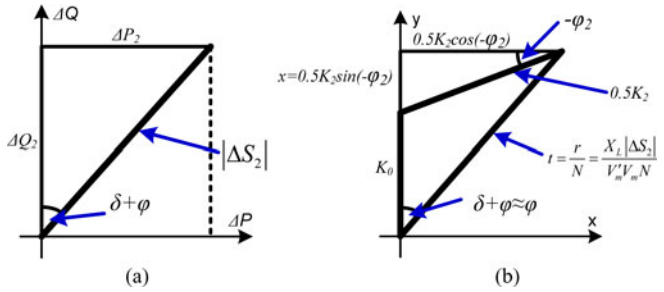

Fig. 6. Minimum power transfer control strategy derivation. (a) Geometric representation for ΔP_2 and ΔQ_2. (b) Geometric relationship between ΔP_2 and ΔQ_2 and K_0, K_2, φ_2.

± 1; from (14) and (15), a maximum control range circle can be plotted in Fig. 5 by varying φ_2. The maximum absolute value of ΔP_2 and ΔQ_2 is 1.43 p.u.

3) $K_0 = \pm 0.5, K_2 \in [-1\ 1], \varphi_2, \in [-\pi\ \pi]$*:* The control range of this condition is between the conditions 1 and 2. The approximate maximum absolute value of ΔP_2 is 0.72 p.u. and ΔQ_2 is 2.15 p.u.

From the previous three examples, it can be concluded that the parameter K_0 mainly affect the ΔQ_2, while the parameter K_2 and φ_2 affect the ΔP_2 and ΔQ_2 at the same time. The overall control range is much larger than the original power flow between the two areas.

C. Minimum Power Transfer Control Strategy Development

A minimum power transfer control strategy is developed in this section. The goal of the strategy is to realize the demanding increment active power and reactive power at the same time, minimizing the power transfer go through the PPCD circuit. This will lead to less power loss and smaller converter size for the PPCD circuit.

Before the analysis, a direct relationship between the control targets ΔP_2 and ΔQ_2 and control variables K_0, K_2, φ_2 are derived to facilitate further calculation. The derivation is under the condition that ΔP_2 and ΔQ_2 are plus. The derivation process will be similar for other conditions. At first, based on (14) and (15), the relations between ΔP_2, ΔQ_2 and $|\Delta S_2|$, $(\delta+\varphi)$ are displayed in Fig. 6(a), where $|\Delta S_2|$ is given as

$$|\Delta S_2| = \sqrt{(\Delta P_2)^2 + (\Delta Q_2)^2} = \frac{r V_m' V_m}{X_L}. \tag{21}$$

Rewriting (21) and comparing with (8), the relations between $|\Delta S_2|$ and K_0, K_2, φ_2 is derived

$$\frac{X_L\,|\Delta S_2|}{V_m' V_m N} = \frac{r}{N} = \sqrt{\left(K_0 + \frac{1}{2}K_2\sin(-\varphi_2)\right)^2 + \left(\frac{1}{2}K_2\cos(-\varphi_2)\right)^2} \tag{22}$$

It is supposed that δ is small enough, which means $\delta+\varphi \approx \varphi$. Then, Fig. 6(a) can be modified to Fig. 6(b) referring to (22) and (9). Fig. 6(b) demonstrates the geometry relationship between $|\Delta S_2|$, $(\delta+\varphi)$ and K_0, K_2, φ_2.

From (2), it can be found that how much power the converter dealing with is decided by the maximum value of D, which is $|K_0|+|K_2|$. Assuming that $M(D) = |K_0|+|K_2|$, the minimum power transfer is achieved when $M(D)$ reaches its minimum value. The function $M(D)$ can be rewritten to (23), where the definition of the variables x and t are given as

$$\begin{aligned} M(D) &= |K_2| + |K_0| = 2\sqrt{[t\sin(\delta+\varphi)]^2 + x^2} \\ &\quad + |t\cos(\delta+\varphi) - x| \\ &= \begin{cases} 2\sqrt{[t\sin(\delta+\varphi)]^2 + x^2} + t\cos(\delta+\varphi) - x\ , \\ \qquad x \le t\cos(\delta+\varphi) \\ 2\sqrt{[t\sin(\delta+\varphi)]^2 + x^2} + x - t\cos(\delta+\varphi)\ , \\ \qquad x > t\cos(\delta+\varphi) \end{cases} \end{aligned} \tag{23}$$

$$\begin{cases} x = \frac{1}{2}K_2\sin(-\varphi_2) \\ t = \frac{X_L\,|\Delta S_2|}{V_m' V_m N} = \sqrt{(K_0 + \frac{1}{2}K_2\sin(-\varphi_2))^2 + (\frac{1}{2}K_2\cos(-\varphi_2))^2}. \end{cases} \tag{24}$$

Differentiate (23) to find the minimum value of $M(D)$; the results are as follows:

$$\min\{M\} = \begin{cases} \sqrt{3}t\sin(\delta+\varphi) + t\cos(\delta+\varphi), & \text{when } \delta+\varphi < 60^\circ \\ 2t, & \text{when } \delta+\varphi < 60^\circ. \end{cases} \tag{25}$$

These results are achieved under the following conditions:

$$\begin{cases} x = \frac{t}{\sqrt{3}}\sin(\delta+\varphi) \Rightarrow K_0 = t\cos(\delta+\varphi) - \frac{t}{\sqrt{3}}\sin(\delta+\varphi) \\ \qquad K_2 = \frac{4}{\sqrt{3}}t\sin(\delta+\varphi),\ \varphi_2 = -30^\circ, \\ \qquad \text{when } (\delta+\varphi) < 60^\circ \\ x = t\cos(\delta+\varphi) \Rightarrow K_0 = 0, K_2 = 2t,\ \varphi_2 = -(\delta+\varphi), \\ \qquad \text{when } (\delta+\varphi) \ge 60^\circ. \end{cases} \tag{26}$$

A more detail calculation can be presented to show how to implement the proposed control strategy. Assuming that in the system, as shown in Fig. 3, the nominal voltage on both sides is 110 kV and the line inductance L is 10 mH. The phase shift before the compensation is 2°. Calculated with (19), the original active power flow is 134 MW. Set the turn ratio N of T_1 to 0.1. It is supposed that the required increment active power ΔP_2 and reactive power ΔQ_2 are 50 MVA and 50 MVA, respectively; referring to the definition in (24), it has $\delta+\varphi = 45^\circ$, $t = 0.367$. According to (26), the duty cycle D can be given as $K_0 = 0.055$, $K_2 = 0.3$, $\varphi_2 = -30^\circ$, $D = 0.055 + 0.3\sin(2\omega t - 30^\circ)$. Since the power rate of the converter is 0.1 p.u., the output power of the converter at this time will be $(0.055+0.3)\cdot 0.1$ p.u. $= 0.0355$ p.u., which is much less than the rated power of the system.

The operation process of the PPCD circuit is given as follows. During the operation, the PPCD will detect the instant power flow and also receive the power flow command from upper side control center. Required incremental active power and reactive power are generated by internal processor, and then, the duty cycle is calculated out based on the command and send to the converter. The aforementioned method is essentially an offline optimal control scheme which widely exists in the power flow control area of the grid.

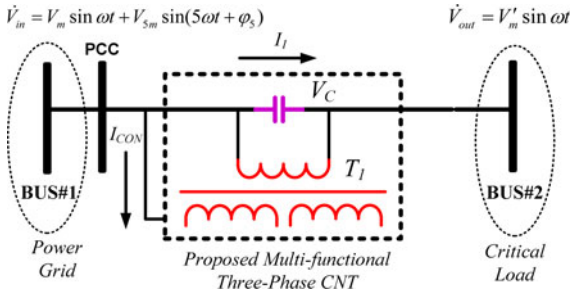

Fig. 7. Typical system with a PPCD circuit for voltage compensation.

IV. Voltage Compensation Method Development and Closed-Loop Control Analysis

The proposed PPCD is also designed to handle the voltage problems in the power distribution system. In this section, the system configuration for voltage compensation is given. Under this configuration, a simple closed-loop control method is realized with the control block diagram displayed, which shows that the system is easy to handle by applying the conventional proportional-integral-derivative (PID) controller.

Fig. 7 shows the system configuration for voltage compensation. $V_{\rm in}$ is the voltage on point of common coupling (PCC), which is distorted by other disturbance sources. For example, $V_{\rm in}$ consists of a fundamental component V_1 with its amplitude V_m and a fifth harmonic component V_5 with its amplitude V_{5m} and phase φ_5 as follows:

$$V_{\rm in} = V_m \sin \omega t + V_{5m} \sin (5\omega t + \varphi_5)\,. \tag{27}$$

The system output is a critical load that requires pure sine input voltage. The expected bus voltage is $V_{\rm out}$ with its rated voltage V_m'. The PPCD is placed between power grid and load. The system shown here is similar with the system for power flow control shown in Fig. 3; thus, the output voltage of PPCD is the same as (1), while $V_{\rm out}$ is expressed by (5) in the system.

A. Voltage Compensation Method Analysis

Take the fifth harmonics elimination and fundamental voltage regulation functions for example. In order to eliminate the fifth harmonic component and regulate the fundamental component to desired $V_{\rm out}$, by applying the DVQS voltage synthesis theory and using the EHM scheme [9], the duty ratio D is given in the form of a dc component K_0 added to a fourth harmonic component with its amplitude K_4 and in phase with the fifth harmonic component in $V_{\rm in}$, which is expressed as follows:

$$D = -\left[K_0 + K_4 \cos\left(4\omega t + \varphi_5\right)\right]. \tag{28}$$

Substituting (27) and (28) into (1), $V_{\rm out}$ can be, then, derived as

$$\begin{aligned} V_{\rm out} &= (V_m \sin \omega t + V_{5m} \sin(5\omega t + \varphi_5)) \\ &\quad \times (1 - N(K_0 + K_4 \cos(4\omega t + \varphi_5))) \\ &= a1 \sin \omega t + a5 \sin 5\omega t + a3 \sin 3\omega t + a9 \sin 9\omega t \end{aligned} \tag{29}$$

where $a1 = (1 - NK_0)V_m - \frac{N}{2}K_4V_{5m}$, $a3 = \frac{N}{2}K_4V_m$, $a5 = (1 - NK_0)V_{5m} - \frac{N}{2}K_4V_m$, and $a9 = -\frac{N}{2}K_4V_{5m}$.

The goal of voltage compensation is to maintain the amplitude of V_1 to $V_m{}'$ and eliminate the amplitude of V_5 to zero. Then, it has

$$a1 = (1 - NK_0)V_m - \frac{N}{2}K_4V_{5m} = V_M' \tag{30}$$

$$a5 = (1 - NK_0)V_{5m} - \frac{N}{2}K_4V_m = 0. \tag{31}$$

In practice, it satisfies $V_{5m} \ll V_m, N < 1, K_0 < 1, N{\cdot}K_0 \ll 1$. So (30) and (31) can be simplified to

$$a1 = (1 - NK_0)V_m = V_M' \tag{32}$$

$$a5 = V_{5m} - \frac{N}{2}K_4V_m = 0. \tag{33}$$

In this two simplified (32) and (33), the control of regulating the fundamental component and eliminating the harmonic components are decoupled. The fundamental component of $V_{\rm out}$ can be adjusted to certain value V_m' by changing K_0, while the fifth harmonic can be eliminated to zero by changing K_4. It means that, despite of the variations in V_m and V_{5m}, a pure sine voltage with desirable amplitude can be synthesized by regulating the duty cycle D of the PPCD circuit.

Generally, in a typical three-phase power distribution system, low-frequency odd-order harmonics such as 5th, 7th, 11th, and 13th are the main harmonics. By utilizing the same method mentioned previously, the 4th, 8th, 10th, and 14th even-order harmonics are added into the modulation wave of the duty cycle D to eliminate the corresponding voltage harmonics in the system.

Similar with the power flow control, the voltage compensation control range is also limited by the duty ratio D, which is expressed as

$$|K_0| + |K_4| + |K_8| + \cdots \le 1. \tag{34}$$

However, it is difficult to plot the control range as Fig. 5 shows for fundamental voltage regulation and harmonics elimination, especially when the system contains various orders of harmonics. According to (1) and (29), an example can show the maximum control range: If $N = 0.3$, the maximum amplitude of fundamental voltage is $\pm 0.3{\cdot}V_m$, while the maximum amplitude of harmonic voltage is $\pm 0.15{\cdot}V_m$.

B. Closed-loop Control Realization

A control architecture, which is based on the parallel form of a DVQS-applied converter, is proposed in [4] and [20] to realize closed-loop control for power factor correction and current harmonic filtering. SRF control theory is employed in the architecture to extract the fundamental component and also the harmonic components in the current waveform. In a similar way, the closed-loop control for the PPCD is proposed to realize fundamental voltage regulation and harmonics elimination function. The control architecture is shown in Fig. 8.

Because the control of the two main functions are decoupled due to former analysis, the control architecture has several

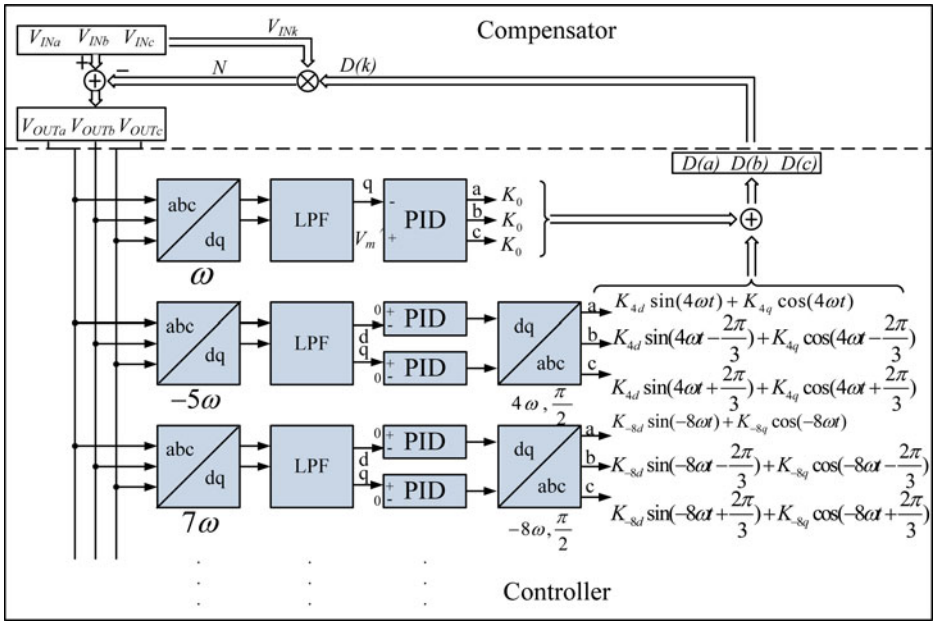

Fig. 8. Closed-loop control architecture within harmonics elimination and voltage regulation.

decoupled control loop including the harmonics elimination loops for each order harmonics and the voltage regulation loop, which is displayed in Fig. 8. In the controller part of the architecture, the three-phase voltage after the compensation $V_{\mathrm{OUT}k}$ is sampled first. In order to extract the amplitude of each *n*th harmonics or fundamental component in $V_{\mathrm{OUT}k}$, Park's transformation is introduced to transform the output "*abc*" voltage to the "*dq*" voltage in each frequency order. This method assumed that the voltage is almost balance. After the extraction, digital low-pass filters are employed to eliminate ac components from the results. The remaining dc components correspond to the amplitude of each order harmonics and the fundamental component in $V_{\mathrm{OUT}k}$. Following that, the outputs from the filters are compared with the references. For the fundamental voltage regulation loop, the value from "*d*"-axis should always be zero and the "*q*"-axis value is compared with reference V_m'. For the harmonics elimination loop, the value from both "*dq*" axes is compared with zero. Taking the reverse-feedback mechanism into account, the input of PID compensator should be connected as Fig. 8 shows. After the comparison, the differences are sent to PID compensators that are utilized to generate the coefficient of *D* in "*dq*" form. Then, the coefficient from harmonics loop in "*dq*" form is transformed to "*abc*" form by applying Ipark's transformation. It should be noticed that particular even-order harmonics are required in duty cycle *D* to eliminate the corresponding odd-order harmonics in $V_{\mathrm{OUT}k}$. Thus, Ipark's transformation matrixes with special frequency and angle are applied in the architecture, which is also given in Fig. 8. Finally, the coefficients in "*abc*" form and the output from fundamental voltage loop are combined together to be the modulation waveform of *D* which is sent to each phase PPCD circuit.

In a typical three-phase power distribution system, assuming that the input voltage is symmetric including the low-frequency odd-order harmonics, such as 5th, 7th, 11th, and 13th, the input voltage can be expressed as shown (35) at the bottom of the next page.

The duty ratio *D* in the three-phase system can be expressed as shown (36) at the bottom of the next page, which is also shown in Fig. 8.

Similar with (5), the output voltage $V_{\mathrm{out}k}$ ($k = a,b,c$) can be then derived as

$$V_{\mathrm{OUT}k} = \begin{bmatrix} V_{\mathrm{OUT}a} \\ V_{\mathrm{OUT}b} \\ V_{\mathrm{OUT}c} \end{bmatrix} = \begin{bmatrix} V_{\mathrm{IN}a} \\ V_{\mathrm{IN}b} \\ V_{\mathrm{IN}c} \end{bmatrix} \cdot \left(1 - \begin{bmatrix} D(a) \\ D(b) \\ D(c) \end{bmatrix} N \right). \tag{37}$$

With the injection of 4th, 8th, 10th, and 14th even harmonics with proper amplitude and phase in the modulation signal, a series of 5th, 7th, 11th, and 13th odd harmonics which has the same amplitude and out phase with the existing harmonics is generated by the compensator and counteracted the existing 5th, 7th, 11th, and 13th harmonics, only left are the fundamental component and residual higher frequency harmonics. The amplitude of the fundamental component is controlled by setting the value of K_0. So the problems such as the voltage sag, the voltage surge, and the voltage undergoing can be handled at the same time.

V. Simulation and Experimental Verifications

In order to verify the effectiveness of the proposed PPCD, the system in Figs. 3 and 7 with the proposed converter is simulated in MATLAB/Simulink. A same power rate prototype is assembled to compare with the simulation for voltage compensation.

A. Power Flow Control Simulation

The simulation system configuration for power flow control is the same as Fig. 3 shows. The specification of the system is V_1: 110 kV, V_2: 110 kV, and $L = 10$ mH. The phase shift between the two bus is $\delta = 2^\circ$. The PPCD circuit is the same

as Fig. 2(b) shows, where the specification is f_s: 10 kHz, C_{in}: 5 μF, C_1, C_2, C_{s1}, C_{s2}: 10μF, L_1, L_2: 1 mH, and C_{comp}: 1 μF.

Calculating with (19), the original active power flow of the system P_{out} is 134 MW. The original reactive power flow Q_{out} of BUS#2 is -2.3 MVAR. Fig. 9 displays the system power flow change by utilizing the PPCD circuit. The settings of the control variables D are also given to indicate the instantaneous power transferred through the PPCD circuit. As shown in Fig. 9, the PPCD is running in standby mode from 0 to 0.2 s. At this time, K_0 and K_2 is zero. The active power flow P_{out} remains unchanged, while the reactive power Q_{out} slightly decrease to -19 MVAR. K_0 changes to 0.5 at $t = 0.2$ s. At this time, Q_{out} increases to 193 MVAR, but P_{out} just increases to 143 MW, which shows that K_0 mainly affects reactive power. At $t = 0.4$ s, K_0 becomes 0 and K_2 increases to 0.5. From the P_{out} and Q_{out} waveform, it can be found that both of them are changed. It proves that P_{out} and Q_{out} can be both determined by varying K_2 and φ_2. During this period, $M(D)_{0.4} = 0.5$, $P_{\text{out}} = 185$ MW, $Q_{\text{out}} = 76$ MVAR. At $t = 0.6$ s, the minimum power transfer strategy is implemented on the PPCD. The P_{out} and Q_{out} have not been changed at this moment, but different values of K_0, K_2, and φ_2 are used. It has $M(D)_{0.6} = |K_2|+|K_0| = 0.433 < M(D)_{0.4}$, which means that the PPCD circuit deals with less power during this time than the time from 0.4 to 0.6 s. The result shows the effectiveness of the minimum power transfer strategy.

Fig. 10 shows the step change waveform of the system active and reactive power flow when the PPCD begins to operate. It can be found that at the time 0.4 s, a compensation voltage V_c is injected by the PPCD. V_c consists of fundamental component as well as the third-order harmonics. The system active and reactive power flow is then changed greatly.

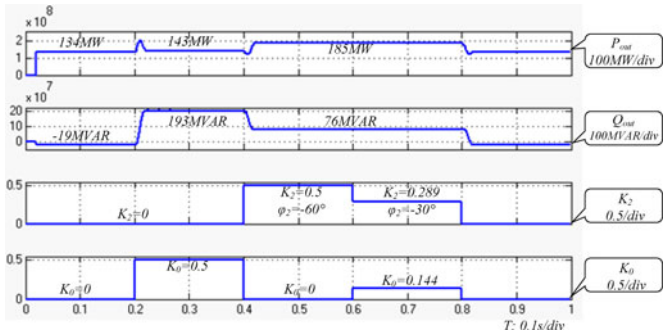

Fig. 9. System power flow change and control variables setting during power flow simulation.

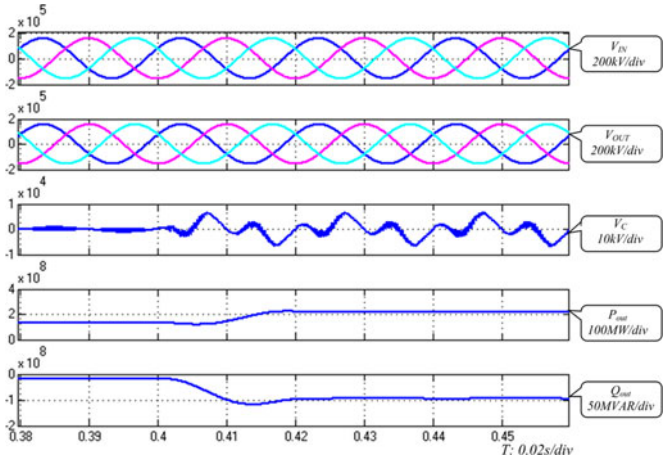

Fig. 10. Step change demonstration of system active and reactive power after applying a PPCD circuit.

$$\begin{bmatrix} V_{\text{IN}a} \\ V_{\text{IN}b} \\ V_{\text{IN}c} \end{bmatrix} = \begin{bmatrix} V_1 \sin\omega t - \sum\limits_{n=5,11,\ldots} (V_{nq} \sin n\omega t + V_{nd} \cos n\omega t) \\ + \sum\limits_{m=7,13,\ldots} (V_{mq} \sin m\omega t + _{md} \cos m\omega t) \\ V_1 \sin(\omega t - \frac{2\pi}{3}) - \sum\limits_{n=5,11,\ldots} [V_{nq} \sin(n\omega t + \frac{2\pi}{3}) + V_{nd} \cos(n\omega t + \frac{2\pi}{3})] \\ + \sum\limits_{m=7,13,\ldots} [V_{mq} \sin(m\omega t - \frac{2\pi}{3}) + V_{md} \cos(m\omega t - \frac{2\pi}{3})] \\ V_1 \sin(\omega t + \frac{2\pi}{3}) - \sum\limits_{n=5,11,\ldots} [V_{nq} \sin(n\omega t - \frac{2\pi}{3}) + V_{nd} \cos(n\omega t - \frac{2\pi}{3})] \\ + \sum\limits_{m=7,13,\ldots} [V_{mq} \sin(m\omega t + \frac{2\pi}{3}) + V_{md} \cos(m\omega t + \frac{2\pi}{3})] \end{bmatrix} \tag{35}$$

$$\begin{bmatrix} D(a) \\ D(b) \\ D(c) \end{bmatrix} = \begin{bmatrix} K_0 + \sum\limits_{i=4,10,\ldots} [K_{id} \sin(i\omega t) + K_{iq} \cos(i\omega t)] \\ + \sum\limits_{j=8,14,\ldots} [-K_{jd} \sin(j\omega t) + K_{jq} \cos(j\omega t)] \\ K_0 + \sum\limits_{i=4,10,\ldots} [K_{id} \sin(i\omega t - \frac{2\pi}{3}) + K_{iq} \cos(i\omega t - \frac{2\pi}{3})] \\ + \sum\limits_{j=8,14,\ldots} [-K_{jd} \sin(j\omega t + \frac{2\pi}{3}) + K_{jq} \cos(j\omega t + \frac{2\pi}{3})] \\ K_0 + \sum\limits_{i=4,10,\ldots} [K_{id} \sin(i\omega t + \frac{2\pi}{3}) + K_{iq} \cos(i\omega t + \frac{2\pi}{3})] \\ + \sum\limits_{j=8,14,\ldots} [-K_{jd} \sin(j\omega t - \frac{2\pi}{3}) + K_{jq} \cos(j\omega t - \frac{2\pi}{3})] \end{bmatrix} \tag{36}$$

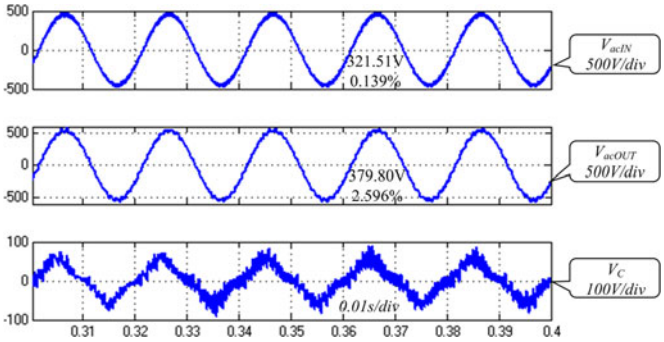

Fig. 11. Simulation result of a system during voltage sag.

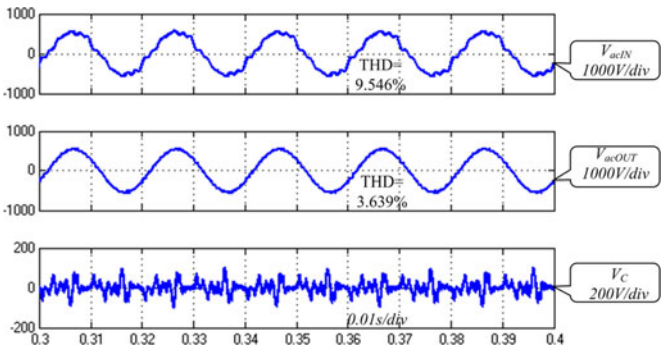

Fig. 12. Simulation result of harmonics elimination.

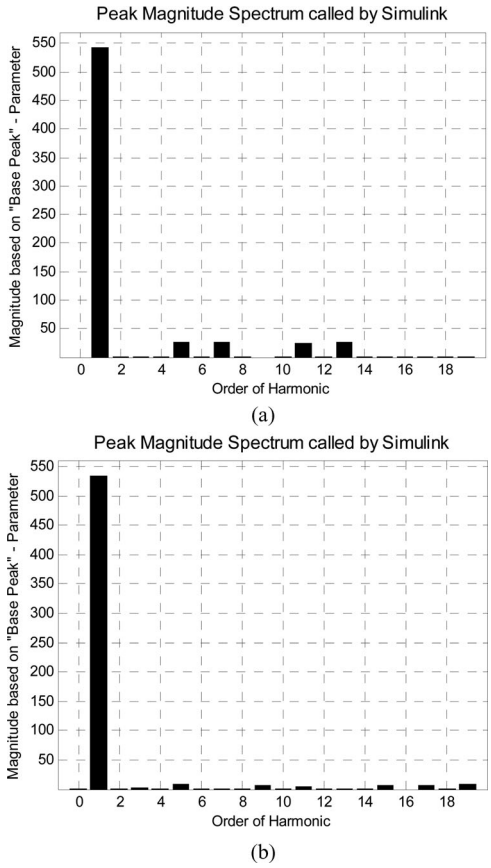

Fig. 13. Harmonics contents comparison between input and output voltage. (a) FFT analysis of V_{acIN}. (b) FFT analysis of V_{acOUT}.

B. Voltage Compensation Simulation

The simulation system configuration for voltage compensation is the same as Fig. 7 shows. The specifications of the system are given by V_{in}: 190–250 V; V_{out}: 220 V; V_{line}: 380 V; P_{out}: 30 kW; f_s: 10 kHz; C_{in}: 5μF; C_1, C_2, C_{s1}, C_{s2}: 10 μF; L_1, L_2: 1 mH, and C_b: 1 μF. The system is designed to eliminate 5th, 7th, 11th, and 13th harmonics with 15% total harmonic distortion (THD) and deals with the 15% voltage sag and voltage swell taking place in V_{in}.

Fig. 11 shows the simulation result of the proposed system during the voltage sag. The input line voltage V_{acIN} fells to 321.5 V during the simulation, which becomes 85% of the rated voltage. The PPCD circuit in each three phase injects a fundamental voltage in phase with the input voltage. As a result, the output line voltage V_{acOUT} remains at rated voltage, which is 379.8 V as shown in Fig. 11. The THD of V_{acOUT} is slightly increased because of low-frequency harmonics caused by switching. This problem can be solved by further applying the harmonics elimination function which is shown in the following.

Fig. 12 demonstrates the operation of the harmonics elimination function. 4.8% of the 5th, 7th, 11th, and 13th harmonics are generated in the input voltage V_{acIN}. Thus, its THD is 9.546% according to the calculation. With the operation of the PPCD circuit, the THD of the output voltage V_{acOUT} is reduced to 3.639% which is much smaller than the input.

Fig. 13 shows the fast Fourier transform (FFT) analysis of the V_{acIN} and V_{acOUT}. It is clear that the 5th, 7th, 11th, and 13th harmonics are all greatly reduced by the operation of the compensator. Although the output voltage still cannot be considered as the pure sine because some uncontrolled harmonics such as 15th, 17th, and 19th order are slightly increased due to the switching operation of the PPCD circuit. The performance can be further improved by adding more control loops in the PPCD circuits to eliminate the higher order harmonics.

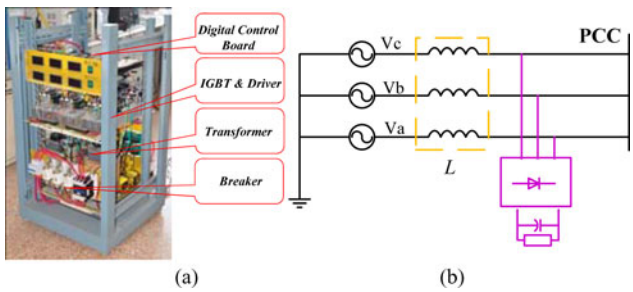

Fig. 14. 30-kW prototype for voltage compensation. (a) Prototype. (b) Schematic of a harmonic generation circuit.

C. Prototype Demonstration

A prototype is designed to verify the voltage compensation function. The specification of the prototype is the same as the voltage compensation simulation model mentioned in Section B. Fig. 14(a) demonstrates the 30-kW prototype. It consists of the digital control board, the PPCD direct ac–ac circuit, the connection transformer, and the breaker.

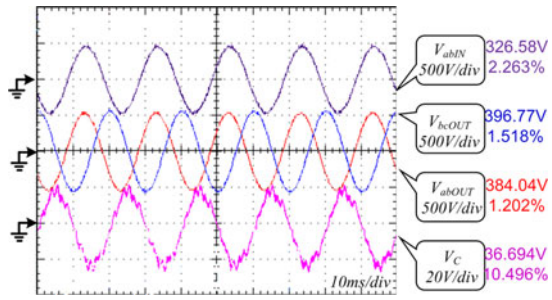

Fig. 15. Experimental results of fundamental voltage regulation.

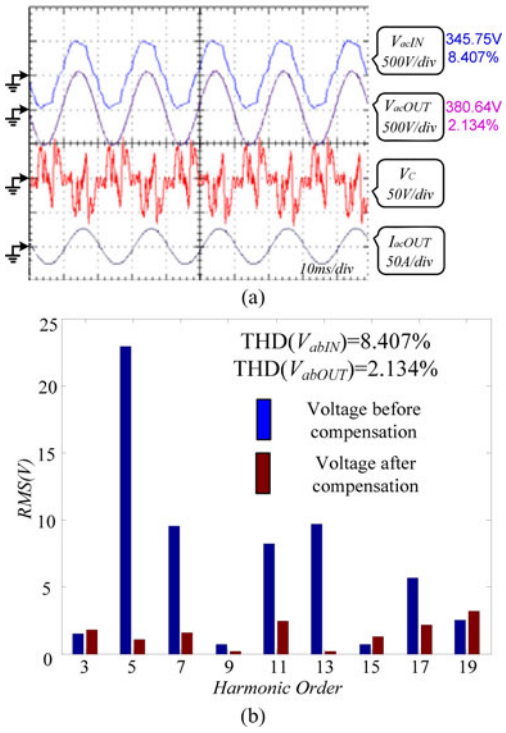

Fig. 16. Experiment results of harmonic elimination. (a) Waveform for harmonics elimination function. (b) Fourier analysis for input and output voltage.

The function of regulating the fundamental voltage is demonstrated by varying the input voltage using an auto-transformer. In order to verify the function of eliminating the harmonic components, an additional harmonic generation circuit is designed to generate the harmonics. The schematic of the circuit is shown in Fig. 14(b). Inductors and diode rectifier are used to simulate the impedance of the transmission lines and nonlinear load in the experiment. The inductance of the inductor is 1.8 mH. The THD of the voltage on PCC can be adjusted by altering the resistor. In the experiment, the total load is 15 kW.

Fig. 15 shows the experimental results of fundamental voltage regulation. From the results, it can be found that despite the variations in the input voltage, the fundamental value of output voltages such as V_{bcOUT} and V_{abOUT} are maintained to about 380 V_{rms}. The THD of the output voltage is smaller than the simulation shows. The reason is that the high-frequency harmonics caused by switching is damped by the wire resistance in the circuit.

Waveform shown in Fig. 16(a) demonstrates the harmonics elimination function and fundamental voltage regulation at the same time. The fundamental RMS value of V_{abIN} is 345.75 V and the THD of V_{abIN} is 8.407%, while the fundamental RMS value of V_{abOUT} is 380.64 V and the THD of V_{abOUT} is 2.134%. Fig. 16(b) displays the results of Fourier analysis for both input and output voltage. It can be found that 5th, 7th, 11th, and 13th harmonics are decreased greatly, while the 15th, 17th, and other uncontrolled harmonics are not increased significantly.

VI. Conclusion

In this paper, a novel PPCD is proposed to realize power flow control and voltage compensation in the three-phase power distribution system. The PPCD circuit is attributed to a direct ac–ac converter, which is derived from a push–pull forward dc–dc converter. It can achieve arbitrary voltage output without any large electrolytic capacitors. Thus, the system reliability can be enhanced. Furthermore, the converter has no full-rated components, which reduces the cost. In this paper, the basic PPCD circuit is introduced first. Next, an injection model along with a minimum power transfer control strategy for power flow control is developed. As a result, the circuit will have the minimum power loss during the operation. Then, the system configuration and the closed-loop control method employing the SRF theory for voltage compensation are developed to enable the precise control. In order to verify the functions, both of the systems with PPCD are simulated by MATLAB/Simulink. Finally, the experiments for voltage compensation are carried out based on a 30-kW prototype, which shows the effectiveness.

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