

30 kW, 200 V/900 V, Thyristor LCL DC/DC Converter Laboratory Prototype Design and Testing

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Abstract—This paper details design, development, and testing of a prototype 30 kW, 200 V/900 V resonant dc/dc converter. The converter achieves stepping ratio of 4.5 without internal ac transformer, and is capable of bidirectional dc power flow as well as fast dc power reversal. Very importantly, it has capability of dc fault isolation on either side, which is of extreme importance for high-power dc applications. The design and selection of the individual passive and active components are presented. A 30-kW test setup including one 900 V voltage source converter (VSC), one 200 V VSC, and one 200 V current source converter (CSC) are designed and built to provide a test rig for dc/dc converter. The analytical studies of efficiency are compared with the converter measured efficiency. The prototype shows overall efficiency of around 92% at full power and weight of around 32 kg, which is promising for scaling to high-power applications. The converter operation at full power in step up mode as well as step down mode, and fast power reversal when connected to CSC on its low voltage side, are demonstrated by experimental results. Severe pole-to-pole dc faults are applied on 900 V and 200 V dc terminals and the inherent dc fault isolation capability is confirmed.

Index Terms—DC/DC power conversion, dc power transmission, efficiency, HVDC converters, resonant power conversion.

I. INTRODUCTION

THERE is currently a lot of interest in developing medium and high-power dc–dc converters for applications as diverse as electric vehicles (20–100 kW) [1], offshore wind turbines (3–6 MW) [2], [3], sub-sea compressors in offshore oil and gas applications (6–80 MW) [4], and high-voltage dc (HVDC) applications (> 100 MW) [5]. Possible technologies include conventional switch-mode-type power supplies (generally limited to low stepping ratio) [2], [6], medium-frequency transformer-based designs [3], [7]–[9], and resonant converters [5], [10].

Despite the large number of markets for dc–dc converters, no technology has achieved widespread application and there is

currently a need for further work both in conceptual design and modeling, as well as in practical testing.

Resonant converters show some promising properties for the high-power, high-voltage applications as they have low converter weight (with no internal ac transformer), high efficiency, can be built with phase control thyristors, capable to link two VSCs or one VSC to one CSC, and have excellent inherent responses to dc faults [5].

This paper reports on developing a bidirectional 30 kW, 200 V/900 V, thyristor LCL dc/dc converter with topology given in [10]. The primary goal of the prototype is to confirm the analytically studied converter capabilities by experimental results. We also aim to demonstrate feasibility of scaling up to a MW sized unit using the proposed topology of [10], rather than fully optimizing the 30 kW design. Therefore, we will select air-core inductors and phase-control thyristors since these components will be required with MW-size converters. Large 1.8 kV/270 A switches are used for 30 kW prototype converter, which are indicative of the technical properties with MW-size technologies.

A complete test rig including one 200 V VSC, one 900 V VSC, and one 200 V CSC all with 30-kW power rating needs to be designed, developed, and fully tested. The aim is to demonstrate prototype dc/dc converter at full power in step up and step down modes linking either 200 V VSC or 200 V CSC to 900 V VSC as well as feeding a high-power resistive load from a firm dc voltage provided by either VSCs or CSC. The test rig also requires robust dc fault hardware in order to demonstrate very low impedance dc faults across the dc/dc converter terminals while it is feeding full power in either step up or step down mode.

We will also analyze prototype losses in some depth and in particular, the low voltage (LV) side inductors and reverse recovery losses, which cause major design challenges. The thyristors will have large reverse recovery currents and overvoltage spikes at higher operating frequencies and suitable passive RC snubbers are required to limit the switch overvoltage spike caused by inductors stored energy at the reverse recovery current snap off. The snubber design is studied in Saber simulator, and tested on the prototype hardware. The converter loss model is developed in MATLAB and the results are compared with detailed measured efficiency results obtained in several experimental tests.

Section II of this paper outlines the design of the converter and general component sizes. Section III details the high-frequency high-power inductor and capacitor design we need for resonance circuits. Section IV addresses the laboratory built dc grid. The prototype dc/dc converter experimental test results are demonstrated and discussed in Section V. Section VI shows the converter efficiency analysis.

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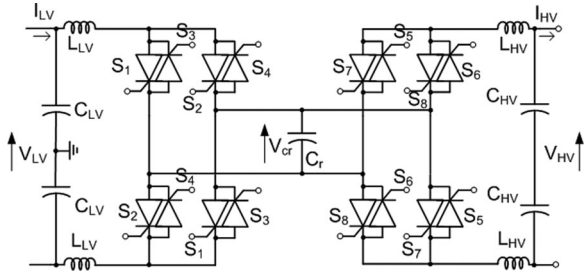


Fig. 1. LCL thyristor bidirectional dc/dc converter (type II). Type I is obtained if LV side thyristors (S_3-S_4) are removed.

II. CONVERTER DESIGN

A. Introduction

Fig. 1 shows the bidirectional LCL thyristor-based high-power dc/dc converter described in depth in [10]. Only a summary is given in this section. It consists of two resonant LC circuits, back-to-back connected and sharing a common capacitor C_r in the middle. This topology uses two symmetrical thyristors in each valve and achieves fast power reversal by reversing dc currents on high voltage (HV) and LV side (type II). A unidirectional version would have half the switches [10]. It can also be used for fast bidirectional power flow with current direction change on HV side whereas voltage polarity change on its LV side in which case LV side has half the switches (type I). Type I might be suitable in connecting CSC converters (HVDC or drives) to a fixed dc polarity dc grid.

In step up mode, the S_1 and S_2 thyristor pairs are sequentially fired at 50% duty ratio at f_s switching frequency, which is the converter control input. The inductor L_{LV} creates a resonance with C_r which enables V_{cr} voltage increasing and provides zero-current turn ON and OFF for S_1-S_2 .

All the switches should have reverse blocking capability but circuit topology provides current commutation and therefore thyristors are suitable. The high-voltage side resonance circuit ($L_{HV}-C_r$) enables zero current switchings of S_5-S_6 thyristor pairs. In step down mode, the operating principle is similar, but S_3-S_4 and S_7-S_8 thyristor pairs are employed instead (type II). If type I is used in step down then S_1 and S_2 are fired but V_{LV} reverses polarity.

The HV circuit is synchronized to operate at same frequency f_s , but there is freedom in choosing firing angle for S_5-S_8 ($\alpha_{\text{step-up}}$ for step up and $\alpha_{\text{step-down}}$ for step down). The HV inductors (L_{HV}) are smaller than L_{LV} ones, and less critical for the operation. The converter has the capability of input current inherent reduction in the case of severe dc faults on either side [5].

B. 30-kW Converter Design

The design of the converter is based on solving a system of nonlinear equations (derived in [10]) to achieve the following specifications:

- 1) maximum power flow of 40 kW (overrated for control flexibility);
- 2) voltage stepping ratio of 4.5 (200 V/900 V);

TABLE I
CONVERTER PASSIVE COMPONENTS ($f_s = 580$ Hz)

	Size	Component Stress
LV Inductor (L_{LV})	450 μ H	500 $V_{\text{pk}}/175A_{\text{ave}}/100A_{\text{rms}}, 1160$ Hz
HV Inductor (L_{HV})	224 μ H	250 $V_{\text{pk}}/33A_{\text{ave}}/37A_{\text{rms}}, 1160$ Hz
Resonant Capacitor (C_r)	70 μ F	1415 $V_{\text{ACpk}}/220 A_{\text{rms}}, 580$ Hz
LV DC Capacitor (C_{LV})	14100 μ F	100 $V_{\text{DC}}/66A_{\text{rms}}$
HV DC Capacitor (C_{HV})	470 μ F	450 $V_{\text{DC}}/19 A_{\text{rms}}$

- 3) maximum peak-to-peak dc voltage ripple of 5%;
- 4) provide the minimum switch turn-off time for the selected thyristors;
- 5) tolerance for dc faults on the HV side in step-up mode (tolerance for dc faults on LV side in step down mode is inherent [5]).

The prototype power and voltage ranges are chosen based on typical ratings for off-the-shelf high-power phase control thyristor modules. Semikron SKKT 273/18E (1.8 kV, 270 A, 150 μ s) thyristors for the S_1-S_4 and SKKT 57/18E (1.8 kV, 50 A, 80 μ s) for S_5-S_8 are used. Note that the switches have higher current ratings to accommodate switching losses.

The converter is only operated in discontinuous mode to provide zero current and controllable di/dt at switch turn OFF. The initial estimates for the component sizes can be obtained using the following simplified equations for the maximum converter power P_{max} and switching frequency $f_{s \text{ max}}$ [10]:

$$f_{s \text{ max}} \cong \frac{\omega_0}{2\pi} = \frac{1}{4 \cdot T_{\text{off min}}} \quad (1)$$

$$P_{\text{max}} \cong \frac{2V_{LV} V_{HV}^2 C_r}{V_{HV} - V_{LV}} 2f_{s \text{ max}} \quad (2)$$

Where $T_{\text{off, min}}$ is the low-voltage side thyristor minimum turn-off time (150 μ s) and

$$\omega_0 = \frac{1}{\sqrt{2L_{LV} C_r}}. \quad (3)$$

The turn-off time is particularly critical during the faults on HV terminal. Using more detailed modeling it can be shown that turn-off time also depends on HV inductors L_{HV} and firing angle $\alpha_{\text{step-up}}$. Maximizing thyristors turn-off time will provide additional safety margin for HV side dc faults and this can be achieved by increasing L_{HV} or $\alpha_{\text{step-up}}$. However, there is a design tradeoff since increasing L_{HV} and $\alpha_{\text{step-up}}$ will lead to higher voltages across the resonant capacitor and could further increase overvoltages during dc faults. The converter modeling during HV side fault demonstrates that turn-off time should meet [5]

$$T_{\text{off}} < \sqrt{L_{LV} C_r} (\alpha_{\text{step-up}} - \pi) + \sqrt{L_{HV} C_r} \frac{\pi}{2}. \quad (4)$$

The component values are finalized on the model developed on PSCAD platform, and the final component sizes and ratings are given in Table I. Note that the dc capacitance is oversized for the required maximum 5% voltage ripple due to component availability at the time of purchase. The components are given for maximum switching frequency of $f_s = 580$ Hz.

TABLE II
THEORETICAL REVERSE RECOVERY LOSS FOR TWO DESIGNS

Design	C_r	L_{LV}	$(di/dt)_{off}$	$P_{loss,rr}$
$f_s=1000\text{Hz}$	$40\mu\text{F}$	$300\mu\text{H}$	$1.8\text{A}/\mu\text{s}$	478W
	$(32\mu\text{F})$	$(380\mu\text{H})$		
$f_s=580\text{Hz}$	$70\mu\text{F}$	$450\mu\text{H}$	$1.2\text{A}/\mu\text{s}$	183W
	$(56\mu\text{F})$	$(650\mu\text{H})$		

C. Switching Frequency Selection

Although (1) gives theoretically maximum switching frequency of 1666 Hz for the 30 kW prototype, a lower nominal frequency is considered to reduce reverse recovery losses.

We have assessed two designs: $f_s = 1000$ Hz and $f_s = 580$ Hz. Table II compares the components and LV side reverse recovery losses $P_{loss,rr}$ for the two designs, considering ideal lossless LC circuit (shown in bracket) and actual LC circuit implemented on the prototype. The capacitor size is directly proportional to the power transfer and therefore the internal loss must be compensated by increasing C_r . Using (3), inductor size is calculated for given frequency and capacitance, and it reduces for larger C_r .

From (2) and (3), both C_r and L_{LV} are inversely proportional to the frequency. At higher frequencies, we expect lower inductor size, which implies proportionally lower inductor loss. Nevertheless, the reverse recovery loss increases much faster with the frequency increase as seen in Table II.

Since, the converter is operated in discontinuous mode, zero current turn OFF is achieved and current derivative is limited by LC circuit. At turn OFF, the current derivative is given by $(V_{HV}+V_{LV})/L_{LV}$, which gives very low values as seen in Table II.

The methodology presented at [11] is employed to calculate peak reverse recovery current from reverse recovery charge obtained from the switch datasheet. It is evident that design at 580 Hz has almost one third the turn-off loss of 1000 Hz design.

Further analysis has shown that capacitor loss is not significantly increasing with frequency and therefore we have finally selected 580 Hz design.

D. Snubber Design

The inductor energy at reverse recovery current snap off causes high overvoltages, which could lead to switch failure. In order to protect the switches, a single RC snubber is designed for the four active LV side switches (and an additional snubber for HV bridge) as shown in Fig. 2. A single snubber design reduces component costs. The snubber parameters are designed based on the methodology presented in [12], and are verified using converter detailed model on Saber platform. The final component sizes are shown in Table III.

While the snubber is effective at reducing overvoltages across the thyristors, it leads to additional losses. Note that:

- 1) There is a design tradeoff between turn-off losses and the switch overvoltage. Reducing the peak overvoltage results in higher losses.

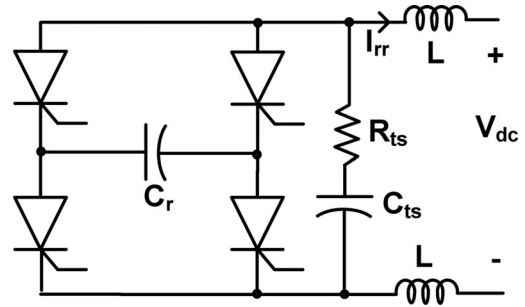


Fig. 2. RC snubber circuit.

TABLE III
RC SHUNT LV AND HV SNUBBER PARAMETERS

	R_{ts}	C_{ts}
LV Snubber	$12\ \Omega$	$440\ \text{nF}$
HV Snubber	$100\ \Omega$	$44\ \text{nF}$

- 2) At turn ON of the thyristors the snubber capacitor will discharge into the resonant capacitor leading to higher di/dt at turn ON and higher thyristor losses (depending on the size of R_{ts}).
- 3) When the thyristors are conducting, the snubber circuit is shunt connected to resonant capacitor C_r , leading to additional losses in the snubber resistor.
- 4) On the HV side, the turn-off losses will be lower because of the lower HV current, and lower reverse recovery charge (smaller switches employed).

III. HIGH-POWER, HIGH-FREQUENCY INDUCTORS AND CAPACITOR

The inductors L_{LV} and L_{HV} are the largest components of the converter and will have significant contribution to the converter total losses. In general, high-power dc/dc converters will require much further development of suitable high-power and high-frequency inductors. The current in inductors in this topology is dc (rectified half-sine) with significant harmonics at $2f_s, 4f_s, \dots$. The primary design goal is loss reduction but the weight and size are also considered.

The inductor losses will depend on the harmonics of the input current and the ac resistance of the inductor and can be evaluated at different power levels using Parseval's theorem

$$P_{loss,L} = \sum_f I_1^2(f) R_{AC}(f) \quad (5)$$

where the rms current I_1 at different frequencies can be evaluated by applying the Fourier analysis on the inductor current. The ac resistance at different frequencies, $R_{ac}(f)$ increases at higher frequency as the result of skin and proximity effects and very few publications exist on theoretical modeling at high power and high frequency. It is measured on prototype using an impedance analyzer.

Four types of inductors are tested on this prototype LV side including: 1) iron core solid-copper dc chokes; 2) air core solenoid using stranded copper cable; 3) air core solenoid using stranded

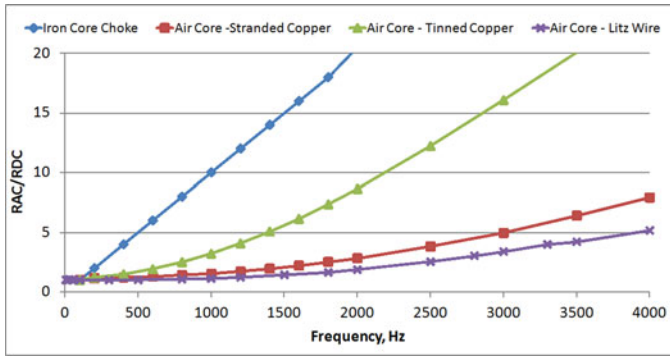


Fig. 3. LV inductor normalized ac resistance.

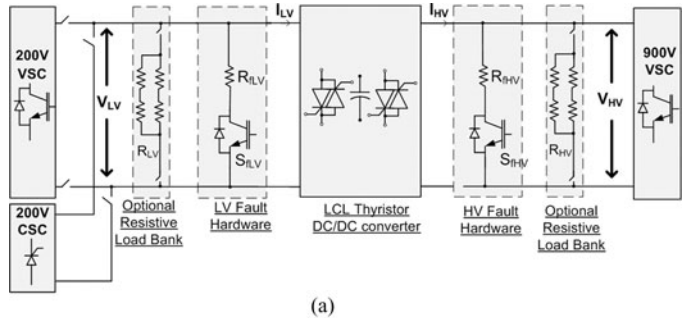
tinned copper cable; and 4) air core solenoid litz wire consisting of 135 strands of 0.63 mm wire (final design). The measured ac resistance for the above inductors versus frequency is shown in Fig. 3 where the base dc resistance, R_{dc} is around 22 m Ω for final design. It is evident that there is very high difference in the ac resistance.

The iron core inductors were built externally, but are clearly unsuitable for high-frequency operation, because of high losses at higher frequencies as seen in Fig. 3. Note that iron core inductors are also subject to saturation at high currents, which might happen for dc faults [5]. The air core solenoid inductors were built in-house using air-core design formulae. The LV inductor dimensions as well as its expected losses at full power are shown in Table IV. The designs with stranded copper and stranded tinned copper wire are identical and use same cables, which are generally interchangeable, except that the latter uses tinned strands. We have observed that the tinned cable has considerably higher ac resistance, which is caused by current concentration at conductor surface (tin) at higher frequencies. It is also observed that the improvement with the Litz wire inductor over the normal stranded copper is less than might have been expected, in particular at frequency range of interest 500–2000 Hz, since the uninsulated stranded wire offers some benefit at reducing the ac losses as discussed in [13].

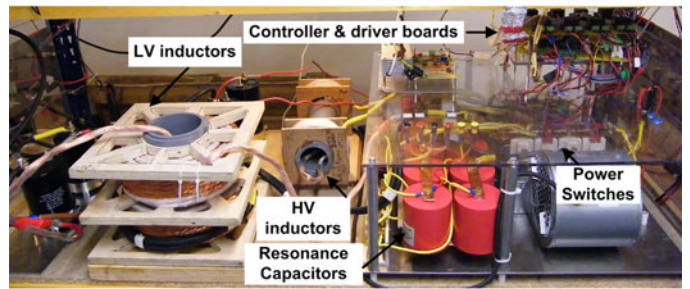
Note that the values shown in Table IV represents a single inductor in isolation. The individual final inductor is of 320 μ H, but we have finally developed two electrically insulated inductors and closely wound as seen in Fig. 4, in order to increase flux which gives total combined inductance of 900 μ H in final design. Observe also that final inductors use densely wound coil ($7 \times 7 = 49$ turns) which gives larger inductance than initial long inductors ($5 \times 14 = 70$ turns).

Two designs for the HV inductors (L_{HV}) are used: the first consisting of solid rectangular copper wire wound around an air core, the second using 45 strands of 0.63-mm Litz wire. The dimensions and estimated losses at full power are shown in Table V. Note that because of the higher harmonics (due to a larger gap between current pulses) on the HV side current of the converter, there is more improvement when Litz wire is used.

The resonant capacitor C_r operates at high frequency (580 Hz in final design and 1 kHz in initial design) and with main ac current but very low harmonics. The current magnitude is directly



(a)



(b)

Fig. 4. Laboratory built test rig. (a) dc grid schematic (b) Prototype dc/dc converter.

dependent on the power transfer level. Commonly, the high-power high-frequency capacitors are used in industry only for snubber applications and for induction heating. The selected ac capacitor C_r is made of an array of film capacitors with dc voltage rating of 1.2 kV, which is derated to maximum 500 V rms for ac voltages. The capacitor ac voltage rating rapidly decreases with frequency increase, but equivalent series resistance marginally decreases. The array was designed for flexibility in experimenting with different sizes and is finally set to two series blocks of four 30 μ F and one 20 μ F capacitors in parallel. The datasheet gives maximum dissipation factors of 3×10^{-4} for the 20 μ F type and 5×10^{-4} for the 30 μ F. Therefore, the maximum ESR of each 20 μ F, and 30 μ F capacitor would be respectively 4.11 and 4.6 m Ω at 580 Hz.

IV. LABORATORY TEST PLATFORM AND DC/DC CONVERTER

A special dc test rig including one 200 V VSC, one 900 V VSC, one 200 V CSC, and one 200 V/900 V LCL thyristor-based resonant dc/dc converter all having 30 kW nominal power has been designed, built, and tested in the laboratory in order to test dc/dc converter in a range of possible applications. On the LV side, the dc/dc converter can be connected to 200 V VSC, 200 V CSC, or 1.3 Ω /30 kW resistive load (R_{LV}). On the HV side, the converter is connected to 900 V VSC emulating a stiff dc grid or 26 Ω /30 kW resistive load (R_{HV}).

The three 30-kW ac/dc converters are built in house and are connected to three-phase 415 V grid voltage via ac stepping transformers, in order to provide the required dc voltage level. Each one of these high-power converters are independently controlled using a F28335 TI microcontroller (150-MHz clock speed, 16 analog inputs, 88 digital IOs, and allows floating

TABLE IV
LV INDUCTORS DIMENSIONS AND TOTAL EXPECTED LOSSES

	Inductance	Core Dia.	Layers x Turns per Layer	Copper Area	Estimated Losses	Weight
Air Core – stranded copper (initial design, $f_s=1kHz$)	250 μ H	115 mm	5 x 14	35 mm ²	2.8%	12 kg
Air Core – stranded and tinned copper (initial design, $f_s=1kHz$)	250 μ H	115 mm	5 x 14	35 mm ²	5.2%	12 kg
Air Core -135x 0.63 mm Litz (Final design, $f_s=580Hz$)	320 μ H	115 mm	7 x 7	42 mm ²	2%	13 kg

TABLE V
HV INDUCTORS DIMENSIONS AND TOTAL EXPECTED LOSSES

	Inductance	Core Dia.	Layers x Turns per Layer	Copper Area	Estimated Losses	Weight
Air Core – solid copper	220 μ H	65 mm	5 x 15	15 mm ²	4%	4.3 kg
Air Core - Litz 45x0.63 mm	220 μ H	75 mm	7 x 7	14 mm ²	0.2%	2.8 kg

point arithmetic) and can be run in dc voltage or current/power control. An Agilent analog card is used to provide coordinated dc grid control at highest level using LabView program running on one computer.

Each converter is equipped with a range of voltage and current sensors where we use LEM HAIS hall-effect-based current sensors and LEM LV 25-P voltage transducers. Because of dc side experimenting, each of these high-power converters has overcurrent protection, which trips grid side ac contactors in the event of fault. The converters are designed to operate through dc faults applied on dc/dc converter terminals with no ac contactor trip (as no very high current is observed during such fault).

VSCs employ outer dc voltage control loop with independent active and reactive ac current inner loops. The switching frequency of 200 V VSC and 900 V VSC is respectively set at 10 and 1.5 kHz. The 200 V VSC uses higher frequency to reduce ac filter size and employs RCD snubbers, which protect insulated gate bipolar transistors (IGBTs). LCL filters are used on ac side to reduce harmonics penetrating to the grid.

The current source converter (CSC) also uses dc voltage control outer loop with inner dc current control loop to provide fault tolerance against dc bus short circuit. Minimum extinction angle control loop is also designed to protect the converter in inversion mode against commutation failure. RC snubbers are employed across each individual thyristor. Fifth and seventh harmonic filters are placed on the grid side, which will also provide reactive power at grid frequency. Smoothing reactors as well as high pass filters are put on the converter dc side.

A simplified dc grid schematic as well as photograph of the dc/dc converter are shown in Fig. 4.

Two low impedance dc fault hardwares have been also designed and built to apply the dc fault on either 200 V or 900 V dc bus. A 1.2 kV, 683 A IGBT (SEMiX453GAR12E4s) in series with small fault impedance ($R_{fHV} = 1 \Omega$ on the HV side and $R_{fLV} = 50 \text{ m}\Omega$ on LV side) is developed. Since transient dc

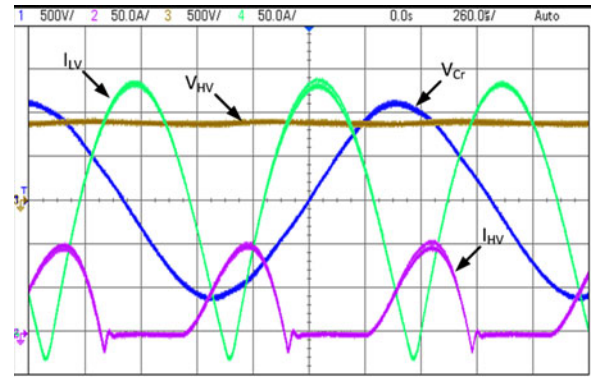


Fig. 5. Steady-state test results for step up mode of operation. $V_{LV} = 200 \text{ V}$, $V_{HV} = 900 \text{ V}$, $f_s = 580 \text{ Hz}$. V_{HV} , V_{Cr} : 500 V/div., I_{HV} , I_{LV} : 50 A/div.

faults are studied, a RC snubber ($R = 20 \Omega$, $C = 220 \text{ nF}$) is used across the IGBT to protect the switch at turn-off instant.

V. DC/DC CONVERTER TESTING

A. Steady-State Operation in Step Up Mode

The converter is tested for power export from 200 V VSC or 200 V CSC to 900 V VSC. The test results obtained for 200 V VSC connection to 900 V VSC through dc/dc converter at 30 kW output power in step up mode are shown in Fig. 5. It is confirmed that the converter operates close to the border with continuous mode, which gives optimal design. Reverse recovery current on both the LV and HV thyristors (in particular on the LV side) is clearly observed.

Detailed experimental study confirmed the optimum firing angle of $\alpha_{\text{step-up}} = 130^\circ$ for HV side thyristors in step up mode in order to maximize LV switch turn-off time during HV side dc faults, while minimizing capacitor C_r peak voltage. The resonant capacitor peak voltage reaches to 1.1 kV, which is well below switch and capacitor voltage ratings.

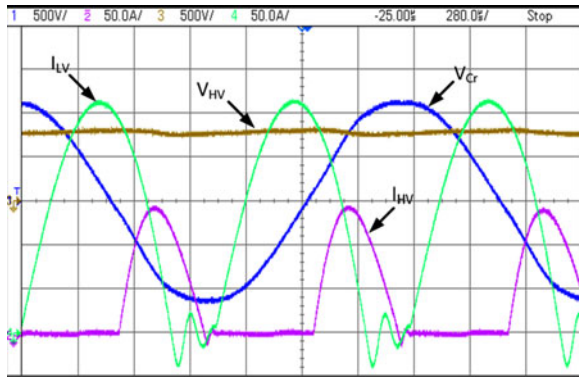


Fig. 6. Steady-state test results for step down mode of operation. $V_{LV} = 210$ V, $V_{HV} = 800$ V, $f_s = 500$ Hz. V_{HV} , V_{Cr} : 500 V/div., I_{HV} , I_{LV} : 50 A/div.

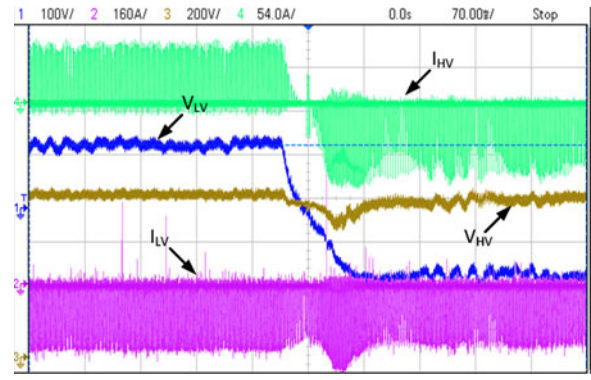


Fig. 7. Power reversal from step up to step down in type I. $V_{LV} = 150$ V, $V_{HV} = 700$ V, $P = 20$ kW. V_{HV} : 200 V/div., V_{LV} : 100 V/div., I_{HV} : 54 A/div., I_{LV} : 160 A/div.

B. Steady-State Operation in Step Down Mode

Fig. 6 shows the test results in which the dc/dc converter is connected to 900 V VSC on its high voltage side and is exporting 30 kW power to a passive LV 1.3 Ω resistive load. This figure confirms capability of dc/dc converter to drive a passive load and further tests with active LV-side dc voltage have been completed. The high-voltage side thyristors firing angle in step down mode is set to $\alpha_{\text{step-down}} = 90^\circ$. Since a resistive load is employed in this test (and difficulties in obtaining exact resistance at required power), the HV VSC is operated at 800 V and the maximum operating frequency has been limited to 500 Hz to avoid LV side voltages larger than 220 V. The oscillations on LV side current at the switch reverse current snap off are caused by the RC snubber in series with L_{LV} . The capacitor peak voltage reaches to about 1.2 kV (generally somewhat higher than in step up operation), which is well tolerated by the selected switches and capacitors.

C. Fast Power Reversal

The capability of the LCL thyristor dc/dc converter in fast power reversal is important in many applications. It is accepted that HV side will generally have constant dc voltage polarity (dc grid), and therefore dc/dc converter provides current reversal.

On LV side, the dc/dc converter can change either current direction or voltage polarity depending on the application. The topology with current reversal on LV side is simpler to design and implement (type II).

In this paper, we report on the capability of fast power reversal by changing voltage polarity on LV side and current direction on the HV side (type I). A typical application would be integration of CSC-based dc systems to VSC-based dc systems. This configuration in fact requires less power electronics on the dc/dc converter, but is more challenging, since power reversal on dc/dc converter must be synchronized with voltage polarity reversal on CSC source (similar as power reversal on thyristor HVDC systems).

Figs. 7 and 8 show the test results for type I fast power reversal on 30 kW prototype. The results are obtained for dc/dc converter linking 200 V CSC to 900 V VSC. Note that the dc/dc converter is operated in closed loop with the LV side dc power regulation. A communication link has been provided between dc/dc con-

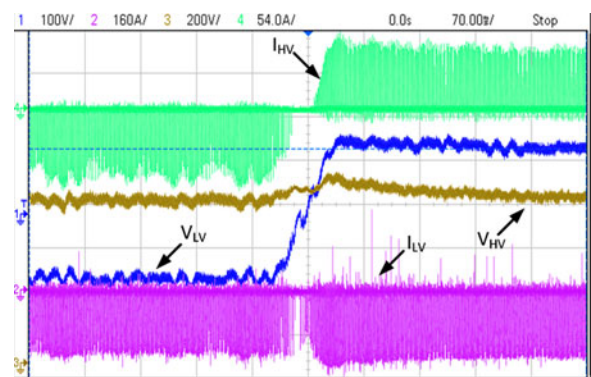


Fig. 8. Power reversal from step down to step up in type I. $V_{LV} = 150$ V, $V_{HV} = 700$ V, $P = 20$ kW. V_{HV} : 200 V/div., V_{LV} : 100 V/div., I_{HV} : 54 A/div., I_{LV} : 160 A/div.

verter and CSC, which is only required to initiate power reversal between the two converters and needs only a digital signal transfer (similar to power reversal process on classic HVDC). The dc/dc converter changes its mode of operation as soon as the reference power signal from LabView changes sign. In this instant, the dc/dc converter controller stops triggering HV side switches (which are conducting), and initiates firing of the reverse HV side switches with different firing angle (see Fig. 1). Following power reference signal sign change, the CSC starts changing the dc voltage polarity. Note that a proper sequence of the firing signals must be generated during power reversal to maintain a successful transient. The results show that HV side current changes its direction whereas the LV side voltage changes its polarity during power reversal, and the whole process takes no longer than 100 ms. A transient voltage drop (or overvoltage) less than 15% is observed on HV side voltage during the fast power reversal. These results also confirm small signal stability and transient performance when a dc grid is operated with three large converters (a VSC, a CSC, and a dc/dc) with independent feedback controls and through large power swings.

D. DC Faults

The LCL dc/dc converter offers excellent property of dc fault inherent isolation from either side [5]. This is of extreme

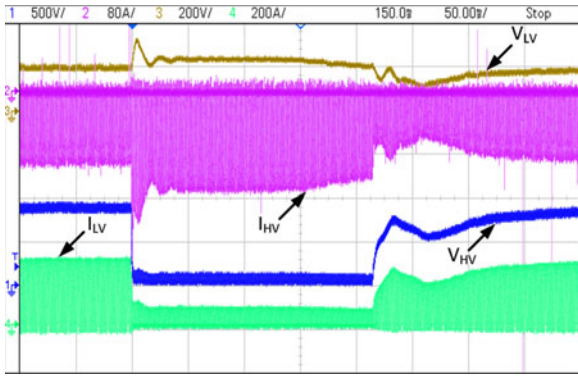


Fig. 9. HV side dc fault response. $V_{LV} = 200$ V (from CSC), $f_s = 580$ Hz. $V_{HV} : 500$ V/div., $V_{LV} : 200$ V/div., $I_{HV} : 80$ A/div., $I_{LV} : 200$ A/div.

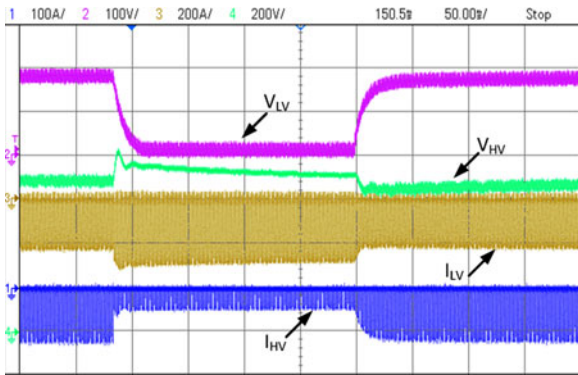


Fig. 10. LV side dc fault response. $V_{HV} = 700$ V (from HV VSC), $f_s = 580$ Hz. $V_{HV} : 200$ V/div., $V_{LV} : 100$ V/div., $I_{HV} : 100$ A/div., $I_{LV} : 200$ A/div.

importance for high-power dc applications in particular since high-power dc circuit breakers are not commercially available.

We have applied transient dc faults while the converter is feeding a 30 kW resistive load. The converter response to dc faults on HV side (in step up operation) and LV side (in step down operation) are respectively shown in Figs. 9 and 10. Note that the converter is in open loop control ($f_s = 580$ Hz) in order to demonstrate inherent response, and further control can additionally improve responses. The slow LV side voltage drops to zero in Fig. 10 when the fault is applied as a result of large filter capacitors C_{LV} employed on this side of the converter.

The results confirm that the fault is not propagated to the other side, and the unfaulted side sees load rejection. The converter normally operates through faults and regains its normal power level after the fault is removed. Note that the faulty side dc current marginally increases, but is still well within the tolerances of the selected thyristors (this can be improved in closed loop operation).

VI. EFFICIENCY ANALYSIS

Fig. 11 shows different losses contribution to the converter total losses obtained from the converter loss model developed in MATLAB. The losses are obtained for two different cases of initial design with maximum switching frequency of 1 kHz and the final converter design with $f_s = 580$ Hz. Using this model, the estimated total loss of the converter is respectively 2012 and

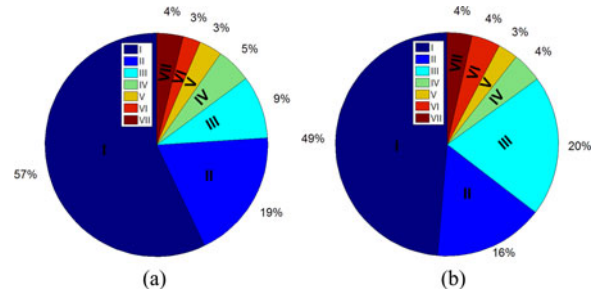


Fig. 11. Prototype theoretical loss study at full power, (a) final design with $f_{smax} = 580$ Hz, Total loss = 2.012 kW. (b) Initial design with $f_s = 1$ kHz, Total loss = 2.345 kW. I: LV side inductor, II: LV side switch conduction, III: LV side switch reverse recovery, IV: HV side inductor, V: HV side switch conduction, VI: HV side switch reverse recovery, VII: Resonant capacitor.

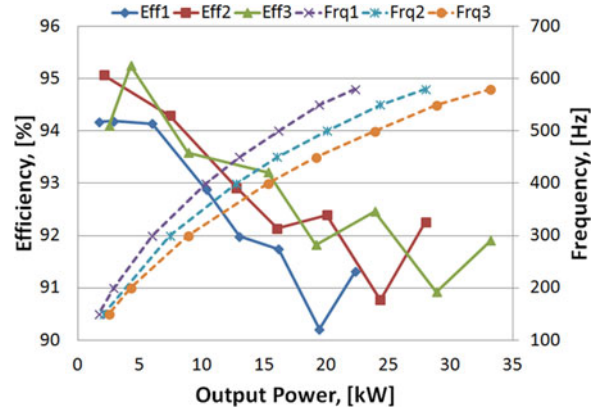


Fig. 12. Measured converter efficiency and converter frequency versus output power in step up mode with resistive load on HV side. 1: $V_{LV} = 180$ V, 2: $V_{LV} = 200$ V, 3: $V_{LV} = 220$ V.

2345 W for maximum switching frequency of 580 Hz and 1 kHz designs.

It is observed that the main sources of losses in this converter include inductor losses (in particular LV side inductor loss) and switch losses.

It is evident that with higher switching frequency, the reverse recovery losses contribution will highly increase but the inductor losses will marginally decrease (smaller inductor is needed). Turn-on losses and off state losses are ignored since the thyristor turn-on transient is very fast and leakage current is quite small.

The converter efficiency is experimentally studied using the laboratory made test rig. The converter is operated in step-up mode in two scenarios: 1) driving a resistive load and 2) supplying a constant dc voltage $V_{HV} = 900$ V and the efficiency curves are shown in Figs. 12 and 13. These figures also depict the converter switching frequency versus output power and show the linear variation of output power versus switching frequency when the HV side voltage is constant. The converter HV side voltage versus switching frequency in step up mode when the converter is connected to 26Ω resistive load on HV side is also shown in Fig. 14. Studying the cases of different V_{LV} in this figure, we can conclude that the converter linearly varies stepping ratio with the frequency input.

The average values of dc voltage and current on either side are measured (using voltage and current meters) for power and

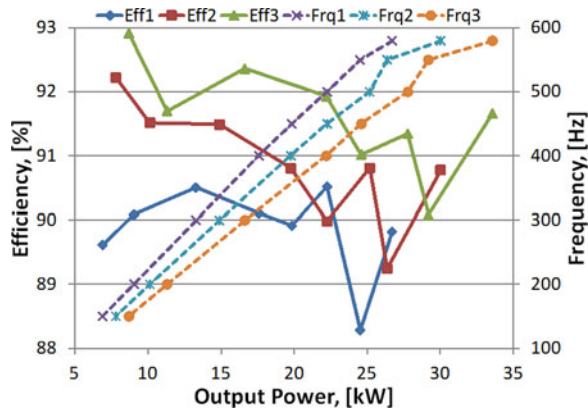


Fig. 13. Measured converter efficiency and converter frequency versus output power in step up mode with firm 900 V dc voltage on HV side. 1: $V_{LV} = 180$ V, 2: $V_{LV} = 200$ V, 3: $V_{LV} = 220$ V.

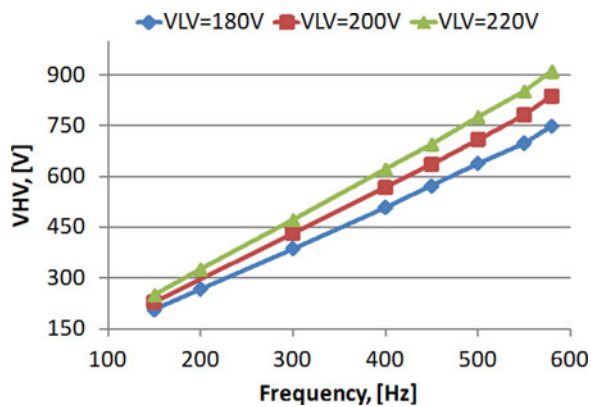


Fig. 14. Measured converter output voltage versus frequency in step up mode with resistive load on HV side.

efficiency calculation. The test is performed for three different LV side voltages of 180, 200, and 220 V in order to analyze impact of stepping ratio. The switching frequency as the converter control variable is varied from 150 Hz to nominal value of 580 Hz in each test.

It is observed that the efficiency marginally decreases while the output power increases. The main reason is reverse recovery losses of the thyristors, which are directly dependent on the switching frequency. In addition, the ac resistance of the inductors increases with switching frequency.

It can be presumed that using fast thyristors, which have lower turn-off losses, we could substantially improve efficiency of this design (using higher switching frequency with smaller inductors). However, largest fast thyristors are in ratings of 2 kV/200 A and while suitable for 30 kW applications they would not be adequate for higher (MW) powers.

Note that our efficiency calculation is subject to a small error in instruments because of high harmonics and magnetic interference from high current air-core inductors. In addition, the LV side inductors have a large thermal resistance, implying different resistance at different tests and difficulties with temperature measurements on internal layers.

It is evident that for higher LV side voltages, higher efficiency is obtained, which is expected as the result of lower LV side

current magnitude for the same power level. We expect that this topology would give best efficiencies for stepping ratios 2–3 (estimated 96.1% for stepping ratio of 2, 200 V/400 V, 30 kW).

Comparing the two efficiency results shown in Figs. 12 and 13, it can be seen that the converter efficiency is marginally larger when it is feeding resistive load. When feeding a passive load, the output power is proportional to square of load current, and the load current itself is proportional to switching frequency, and this implies lower switching frequency for a given output power. As the converter output power increases, the resistive load voltage increases and approaches to 900 V, thus closer efficiency results are obtained.

The efficiency of the converter reaches up to 92% at full power for stepping ratio of 4.5, which is acceptable for this range of power. The commercialized 20 kW boost dc/dc converter discussed in [1] shows the efficiency of 96.7% at full power for stepping ratio of less than 2 (230 V/454 V). Note that more than 50% of our converter total losses come from LV side inductors carrying 175-A average current in full power. This is almost double the current rating of studied Toyota Prius dc/dc converter.

VII. CONCLUSION

A prototype 30 kW, 200 V/900 V LCL thyristor-based resonant dc/dc converter is designed, built, and tested. A 30-kW dc test rig including two VSCs and one CSC is designed, and built to test the prototype dc/dc. The prototype is tested in interfacing either 200 V VSC to 900 V VSC or 200 V CSC to 900 V VSC or these converters with resistive loads. DC/DC converter full power test in step up mode, and step down mode, fast power reversal within 100 ms between 900 V VSC and 200 V CSC are demonstrated. The dc faults are applied on either side of the prototype and confirm all the predicted fault-isolation properties of this topology. The converter full-power efficiency reaches to up to 92%, while at partial loading efficiency is better, which are reasonable values for this range of power and voltage stepping ratios. Work is ongoing to further improve the efficiency using fast thyristors, gate turn-off thyristors, or insulated gate commutated thyristors as the converter main switches, to optimize snubber circuits including lossless snubber design, and to improve high-power high-frequency inductor design.

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