Rapid Prototyping Tools for Power Electronic Systems: Demonstration With Shunt Active Power Filters

Joep Jacobs, *Student Member, IEEE*, Dirk Detjen, *Student Member, IEEE*, Claus-Ulrich Karipidis, and Rik W. De Doncker, *Fellow, IEEE*

***Abstract*—This paper presents three new rapid prototyping tools to develop power electronic systems. The effectiveness of these tools is demonstrated by designing and building a shunt active power filter.**

First, a digital signal processor (DSP) model to embed complex control algorithms has been created for detailed offline simulations with PSpice. This DSP model emulates the discrete behavior of digital control circuits. The control algorithms in the DSP model are implemented in C-code. Secondly, the control C-code can be downloaded to the ISEADSP for real-time execution. The ISEADSP is a universal DSP control board based on two 80 SHARC processors which execute control algorithms of various nature and highest complexity at 80 MFLOP per second. Thirdly, power electronic building blocks (PEBBs) based on IGBT devices were developed to build and analyze quickly different converter topologies. Combining these three rapid prototyping tools led to a significant reduction of development time of power electronic applications.

***Index Terms*—DSP, IGBT, ISEADSP, PEBBs.**

I. Introduction

SO FAR, many rapid prototyping tools have been developed specifically for microelectronic and electronic applications. Few attempts have been made to develop rapid prototyping tools for power electronic systems. Therefore, three projects were initiated to develop power electronic rapid prototyping tools. First, a C-code link was created within the PSpice circuit simulator environment to simulate the discrete time behavior of digital circuits and to emulate all interface circuits of a target digital signal processor (DSP) control board [1], [2]. Secondly, a high performance multi-functional DSP board (ISEADSP) was designed and built specifically for power electronic applications to enable real-time execution of C-code programs. In the third project, power electronic building blocks (PEBBs) were defined and built for fast implementation of various power converter topologies. Finally, another important goal was to demonstrate that the combined use of all three tools would generate synergy, offering the user a flexible and more powerful design environment.

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J. Jacobs, D. Detjen, and R. W. De Doncker are with Institute for Power Electronics and Electrical Drives (ISEA), RWTH-Aachen University, Aachen D-52066, Germany (e-mail: jj@isea.rwth-aachen.de).

C.-U. Karipidis is with Siemens AG Transportation Systems, Erlangen, Germany.

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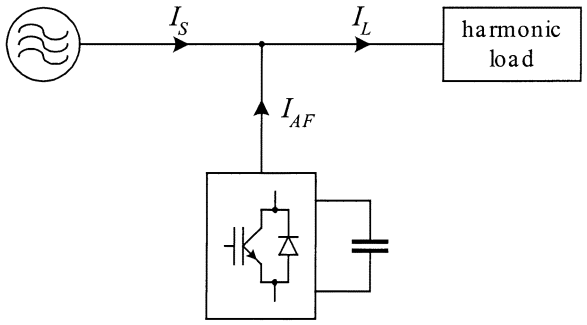

Fig. 1. Principle of a shunt active power filter (SAPF).

As an example, the development of a shunt active power filter (APF) has been chosen to demonstrate the capabilities of these tools. Fig. 1 depicts the principle of the shunt active filter which is being used to compensate harmonic currents generated by nonlinear loads. A demonstrator of the shunt active power filter has been designed and built in less than six months.

The complete topology was first simulated in detail using the simulation environment PSpice. The discrete behavior of the DSP control board was emulated with the PSpice DSP-model using the C-code of the APF controller. The complex algorithms which are required to control the active power filter were tested thoroughly in the PSpice environment. After simulating all operating conditions the control algorithms were downloaded to the ISEADSP for real-time execution and final tests of the APF. A three-phase converter which is the power part of the active filter was built using PEBBs.

These new rapid prototyping tools are highlighted in the following section. Section III describes the shunt active power filter. The control strategies are discussed in detail. Sections IV and V show the simulation and experimental results, respectively.

II. Rapid Prototyping Tools

A. Discrete Digital Control Algorithms in PSpice

The simulation environment PSpice AD is a well suited circuit analysis software for power electronic applications. Using implicit integration, the convergence stability for complex circuitry and the accuracy of PSpice is significantly more reliable compared to explicit integration tools [17], [18]. In addition, several physics based models of power electronic devices such

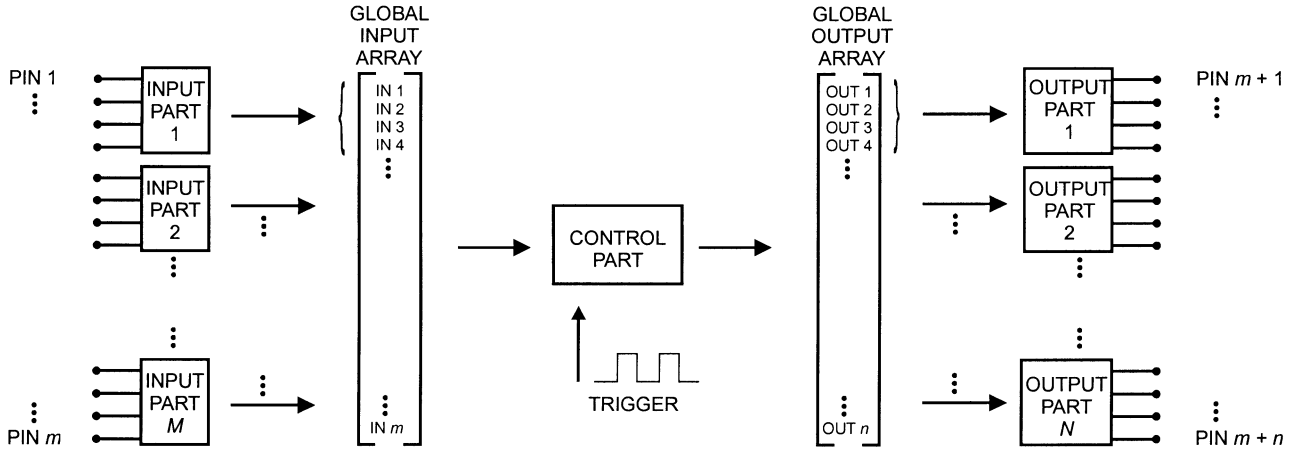

Fig. 2. Internal structure of the DSP model.

as IGBT; psn power diodes and GTOs etc. have been developed for PSpice [1], [15], [16]. With the help of these models, power electronic circuitry can be pre-designed in the simulation software taking into account all important physical effects such as diode recovery behavior, transient switching characteristics of active devices and parasitic components (stray inductances and stray capacitance).

The rising complexity of power electronic applications and their control techniques require an increasing use of microcontrollers and digital signal processors (DSPs). Unfortunately, PSpice does not offer any tools suited to directly simulate these time discrete devices. To accelerate the process of prototyping, circuit analysis software is desirable which achieves simulation of both continuos analog behavior, including the power electronic device physics, and discrete digital behavior of the control circuitry.

The *Device Equation* option of the circuit analysis software PSpice provides the possibility to implement new device models in C-code. New models have to be implemented as submodels of already existing semiconductor models such as MOSFET or DIODE. These semiconductor models solely serve as an interface to the PSpice kernel, i.e., their original meaning as semiconductor device model can be completely ignored. The number of external nodes is limited to four when implementing a new device model as a MOSFET-submodel. This is the maximum number of external pins provided by a PSpice semiconductor model. Due to the large number of in- and outputs normally used for DSP control, a controller model cannot be implemented directly.

Typically, the analog inputs are digitized by means of A/D converters for the digital signal processor system. The DSP processing time, which depends on the processor speed and the number of cycles of the processed program, sets a minimum processing delay prior to changing the outputs. The PSpice kernel uses an adaptive timestep method during detailed transient analysis which is well suited for simulation of analog circuitry. However, the user has generally no control on the calculation instances.

In this section, a method is presented to realize a PSpice model for simulation of DSP systems having analog and digital I/O. An arbitrary number of inputs and outputs can be given to the DSP model although the model is implemented as a MOSFET-submodel. The effects of discrete sampling times and propagation delays caused by the processor can be precisely analyzed. Thus, C-code for the final application can be developed completely in the simulation environment prior to downloading into a real-time target system.

1) Providing an Arbitrary Number of External Nodes: The DSP model is based on the PSpice MOSFET model. The source code of the MOSFET model is part of the *Device Equation* Option. However, the DSP model only uses the MOSFET model as an interface to the PSpice kernel. Depending on the requested number of external pins, a DSP model comprising several MOSFET model parts is generated. Thus, the restriction of a maximum number of 4 external nodes can be eliminated. The model parts can be separated into three types corresponding to their task inside the DSP:

- INPUT parts;
- CONTROL part;
- OUTPUT parts.

According to the number of DSP inputs several INPUT parts are necessary for reading the input signals. As depicted in Fig. 2 every INPUT part writes the voltage potentials of its external nodes into a globally defined array.

The CONTROL part is used to execute the actual C-code of the DSP controlled application. Therefore, it reads data from the previously initialized input array and calculates the corresponding output signals. The results are stored in another global array acting as a buffer. Furthermore, the CONTROL part receives a trigger signal used for time synchronization.

A third MOSFET-type model is used to create an OUTPUT part. It reads data from the global output array and sends these values at the output pins of the DSP model. Furthermore, the OUTPUT parts reinitialize the global output array at every sample with the previously determined values of the buffer list.

2) Time Synchronization: As described in the previous section, the calculation of the DSP model can be divided into three main tasks which have to be executed in a certain order. At every call of the DSP control code the INPUT parts have to initialize first the global input array with the potentials of their external nodes. Next, the CONTROL part uses the values of the INPUT array to determine the corresponding output values and

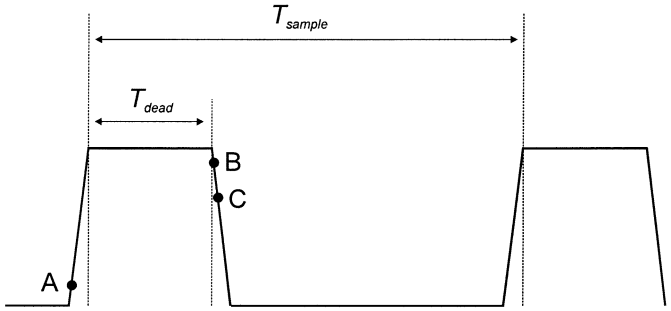

Fig. 3. Trigger signal for fixed time stamped DSP controllers.

stores them in a buffer. Finally, the OUTPUT parts reinitialize the output array with these buffer values. The DSP model comprises several MOSFET parts to execute the described jobs. The activation of these parts is generally unpredictably controlled by the PSpice simulator kernel. To guarantee the required sequence the three tasks have to be executed at different consecutive time steps.

To realize this time discrete behavior a pulse voltage source is connected to the CONTROL part which performs the execution of the DSP control code. This pulse voltage signal acts as a clock signal for the DSP model. Edge triggering is used in the proposed model to initialize the input list, to determine a new output list and to update the DSP output potentials.

Point A in Fig. 3 indicates the first convergent time step at the rising edge of the clock signal. At this time, the input list is initialized. Point B marks the first convergent time step at the falling edge of the clock signal. At this instant the new output values are calculated and written to the new global output list. Exactly one timestep later (point C) the values of the new output list are supplied to the external nodes of the OUTPUT parts. This time delay between calculating the new output values and supplying them to the outputs is necessary to assure that the calculating CONTROL part has been activated by the simulator before each OUTPUT part updates its corresponding output voltage signals. This guarantees that all the output signals of the DSP change synchronously and prevents racing in case algebraic loops are used. At every other simulation time step the INPUT parts and the CONTROL part stay inactive. However, the OUTPUT parts always supply the values of the global output list to their external nodes.

Since PSpice uses an adaptive time step method for transient analysis, it is forced to find at least two convergent time steps on each edge of the voltage pulse. Thus, the scattering of the described time steps A,B,C can be limited by the rise- and fall-time of the voltage pulse.

As Fig. 3 illustrates, the sampling frequency of the DSP-model can be adjusted by the frequency of the pulse voltage source and the propagation delay of the processor can be simulated by the pulsewidth. For every time step the value of the pulse voltage is written to a global cyclically rotating vector with four elements. As a result, every MOSFET part belonging to the DSP model has access to the clock signal over the last four time steps.

The frequency of the pulse voltage source must be initialized by the user at the start of the simulation run by setting the corresponding attribute. It cannot be changed during the simulation run. Hence, the simulation of event driven interrupts or variable timer frequencies are not directly possible in this way. Therefore, the behavior of the pulse voltage source was emulated in C-Code in which parameter variations during simulation runs can be programmed. Its implementation is thoroughly described in [3].

B. Digital Signal Processing System ISEADSP

The ISEADSP board is a development tool for controllers specifically aimed at power electronic and electrical drive applications. To date, several commercial general purpose hardware and software development tools exist to prototype or emulate various applications [4], [5]. Some products are specialized simulators for large, complex systems [6], [7]. However, an approach has not been found that provides a cost-effective but powerful and flexible solution for rapid prototyping and digital real-time simulation of power electronic and electrical drive systems. Therefore, the ISEADSP board was designed according to these goals [8], [9]. Main advantages of the ISEADSP compared to other DSP systems (as for example dSPACE) is the implementation of a hardware synchronization and interrupt configuration network in FPGAs, which enables a highly flexible event driven hardware-configuration. This configuration network allows the DSP to concentrate its calculation power for the control algorithm instead of handling multiple interrupts or hardware-polling tasks. To support this flexibility, all analog channels are configurable to in- or output. Secondly, the ISEADSP board linked to appropriate interface boards is especially designed to avoid EMC problems, when running for example adjacent to fast switching equipment. Lastly, the stand alone operation requires no additional master computer.

The hardware structure shown in Fig. 4 is characterized by the use of powerful digital signal processors (DSPs) offering very high floating-point computing power and separate control interfaces based on flexible field-programmable gate arrays (FPGAs). The FPGAs allow the implementation of many application-specific digital control interfaces. A high number of analog channels was realized using A/D- and D/A-converters with serial digital interfaces. The DSPs are complemented by timers, an interrupt manager (IRQ) and mechanisms to precisely synchronize and manage hardware processes (HWS) of all control interfaces. This structure is expandable to realize an over a large scalable multiprocessor systems.

Complemented by an additional application-specific signal conditioning board the ISEADSP board can be used as stand-alone controller. The extension bus allows to couple up to five ISEADSP boards directly without backplane. Larger clusters are realized though a VMEbus interface allowing up to 20 ISEADSP boards to operate in synchronization.

Fig. 5 depicts the actual ISEADSP board. It is constructed as a VMEbus-compatible U6-size board. It offers up to two floating-point SHARC ADSP-2106x DSPs of Analog Devices. Each ISEADSP board can be equipped with 64 simultaneous sampling memory mapped analog channels. It is an unusual feature to provide all analog channels with individual A/D-con-

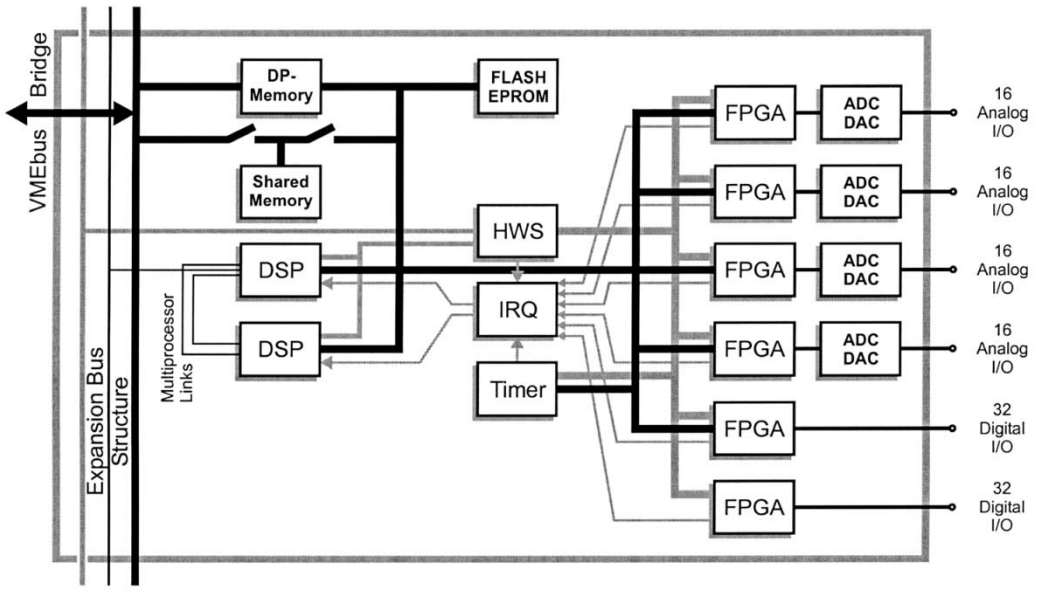

Fig. 4. Architecture of the ISEADSP control board.

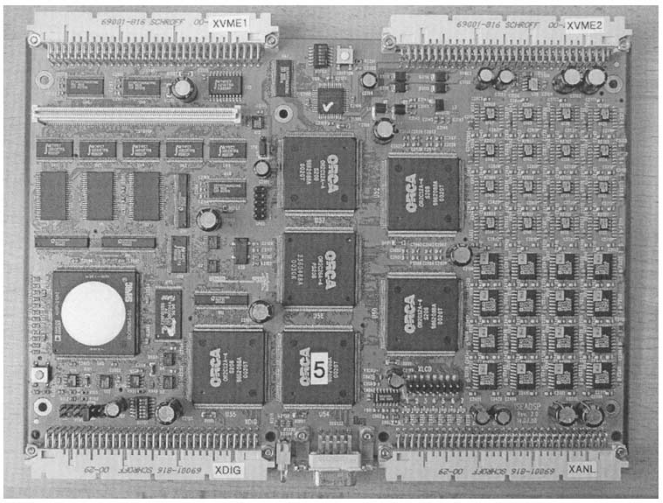

Fig. 5. ISEADSP top view.

verters 139 ksamples, 14-b accuracy or D/A-converters 6 μs settling time, 16-b accuracy. These converters are mounted on both sides at the right hand side of the board as shown in Fig. 5. Two FPGAs implement 64 versatile memory mapped digital channels. A library of firmware provides for, among others, incremental encoder interfaces or up to 32 PWM channels. The surface mounted connectors (noticeable at the left hand side of the board, directly above the shared memory bank) allows direct coupling of multiple DSP boards. This extension bus supports broadcast mechanisms which are essential for real-time simulators.

The ISEADSP board allows to set up software and hardware to application-specific requirements simply by downloading a single file. The ISEADSP excels with regard to flexibility and extensive real-time control resources without loading the DSPs. The advantage of floating point calculations and C-language support makes the board easy to use.

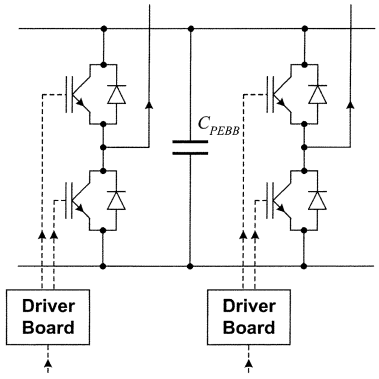

Fig. 6. Standard power electronic building block (PEBB).

C. Power Electronic Building Block (PEBB)

The Power Electronic Building Blocks are static power converters developed for research on electrical drives and power supplies up to 200 kVA [10], [19]. Extensive effort was made to minimize electromagnetic interference (EMI) with a very low inductive design. EMI problems within the converter were eliminated. In addition, the PEBBs became less susceptible to EMI noise of other equipment. Although, the PEBBs are designed to be used in prototype converters (field testing) they provide easy access for voltage and current measurements to allow research on new inverter topologies.

A wiring diagram of the standard PEBB unit is depicted in Fig. 6. The PEBB is realized with two IGBT modules comprising two IGBTs each with anti-parallel diodes. The IGBTs maximum collector-emitter voltage is 1200 V and the maximum collector current is 300 A. The dc link capacitor C_{PEBB} is a film capacitor with 2.2 mF capacitance. The maximum switching frequency f_s of the IGBTs is 20 kHz at 100 kVA and 10 kHz at 200 kVA.

Each PEBB also comprises the IGBT driver boards, the cooling system, monitoring equipment, and a soft-start unit.

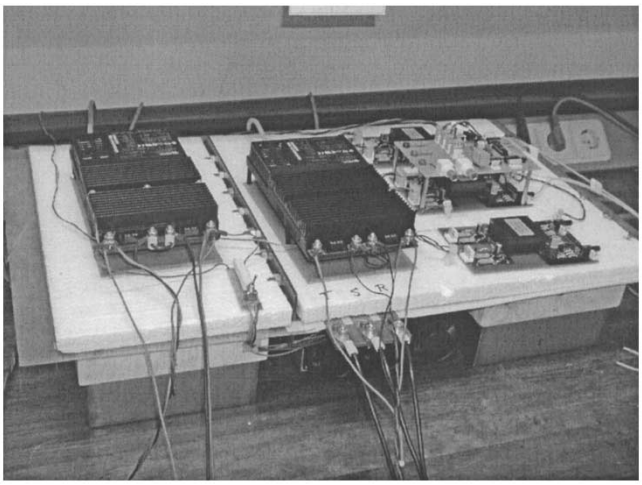

Fig. 7. Three-phase converter with PEBB.

The driver boards are commanded via fiber optic interfaces. The cooling system can either be forced air cooled or a water cooled system. The monitoring equipment measures signals required for control and fault indication. The soft-start unit controls the charging and discharging of the dc link capacitors.

Although PEBB units are primarily constructed with standard parts, the design is flexible enabling reconfiguration. Using two PEBBs a three- or four-phase input rectifier or a three- or four-phase output inverter can be built (Fig. 7). To realize a complete system with a three-phase bridge rectifier and a three-phase output inverter three standard units are required.

III. Shunt Active Power Filter

An increasing number of nonlinear loads in electrical power systems generate medium-frequency harmonic currents. These harmonic currents cause additional heat in power cables, transformers, electrical machines, and capacitors. The system's power factor is reduced because these harmonic currents usually only add to the reactive power flow. Hence, the harmonic currents can induce high harmonic voltages across the source impedance, thereby distorting the supply voltage. This effect can influence or even damage computers or process controllers. Other negative effects of harmonics are current flow in the neutral conductor, flicker effects, loss of power, and extra operating costs.

In the past, different passive and active filter topologies have been investigated [11]–[13] and successfully installed to compensate the harmonic load currents. However, passive filters are far less flexible and limited in use in comparison to active filters [11]. One of the active filter topologies which showed good results is the shunt active power filter. This filter can be used to cancel harmonic currents generated by harmonic loads and/or to compensate reactive power. As a result the shunt active power filter (SAPF) forces the source currents to become almost sinusoidal and/or in phase with the phase voltages

$$I_S + I_{AF} = I_L.$$

A block diagram of the shunt active power filter is depicted in Fig. 8. A three-phase voltage source feeds a harmonic load which consists of a B6-bridge rectifier feeding a resistive-inductive load R and L. The load currents I_{La}, I_{Lb}, and I_{Lc} are measured and sent to the ISEADSP board. The ISEADSP board calculates the harmonic content I^*_{AFa}, I^*_{AFb}, and I^*_{AFc} of the load currents. These signals are sent to a current hysteresis controller, which is chosen for its stability and simplicity. The hysteresis controller determines the pulse pattern and transmits these to the IGBT driver boards. As a result, the power converter injects the filter currents I_{AFa}, I_{AFb}, and I_{AFc} into the power system. The filter coils L_F are needed to smooth the inverter currents.

The underlying goal of the APF study was to compare APF topologies which are capable of compensating unbalanced voltages and voltage harmonics of the three-phase sources. To this end, the three-legged inverter with midpoint connection and the four-legged inverter topology as presented in [14] were compared in detail. The three-legged APF with dc voltage midpoint was selected to verify the rapid prototyping tools. Due to the connection between dc midpoint and neutral wire, the converter is able to inject three independent filter currents. The dc link is free floating, fed by the ac system to which it is connected.

The control part of the shunt active power filter is completely implemented in the ISEADSP. It comprises the synchronization of all signals, the determination of the harmonic content of the load currents, the control of the total dc voltage V_{dc}, and the symmetration of the dc voltages V_{dc+} and V_{dc-}.

A. Synchronization of Reference Signals and Phase Voltages

To synchronize the reference signals with the fundamental components of the first phase voltage, the phase angle θ of the source voltage E_a has to be determined. This phase angle and fundamental frequency f_1 are provided by a phase locked loop (PLL). Therefore, the three phase voltages E_{Sa}, E_{Sb}, and E_{Sc} are measured and the reactive or q-component E_q of these voltages is calculated [14]

$$V_q = \begin{pmatrix} \sin\Theta & \sin\left(\Theta - \frac{2\pi}{3}\right) & \sin\left(\Theta + \frac{2\pi}{3}\right) \end{pmatrix} \cdot \begin{pmatrix} E_{Sa} \\ E_{Sb} \\ E_{Sc} \end{pmatrix}.$$

When the angle θ is equal to the phase angle of the voltage vector, the q-component of the fundamental voltage vector is zero. Hence, by adjusting the angle θ the q-component can be controlled to zero, realizing a tracking of the phase angle of the phase voltages. The control of this synchronization is realized with a digital PI-controller as shown in Fig. 8.

B. Calculation of the Harmonic Content

The harmonic content of the load current is generated with help of the dq-transformation [14]. This method is based on a space vector transformation. The time dependent load currents I_{La}, I_{Lb}, and I_{Lc} are measured in a stationary reference frame and subsequently transformed into the rotating dq-reference frame. The dq-system rotates with the fundamental of the ac supply frequency f_1. The phase angle θ is provided by the PLL as mentioned in the previous section

$$\begin{pmatrix} I_{Ld} \\ I_{Lq} \end{pmatrix} = \frac{2}{3} \begin{pmatrix} \cos\Theta & \cos\left(\Theta - \frac{2\pi}{3}\right) & \cos\left(\Theta + \frac{2\pi}{3}\right) \\ \sin\Theta & \sin\left(\Theta - \frac{2\pi}{3}\right) & \sin\left(\Theta + \frac{2\pi}{3}\right) \end{pmatrix} \cdot \begin{pmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{pmatrix}.$$

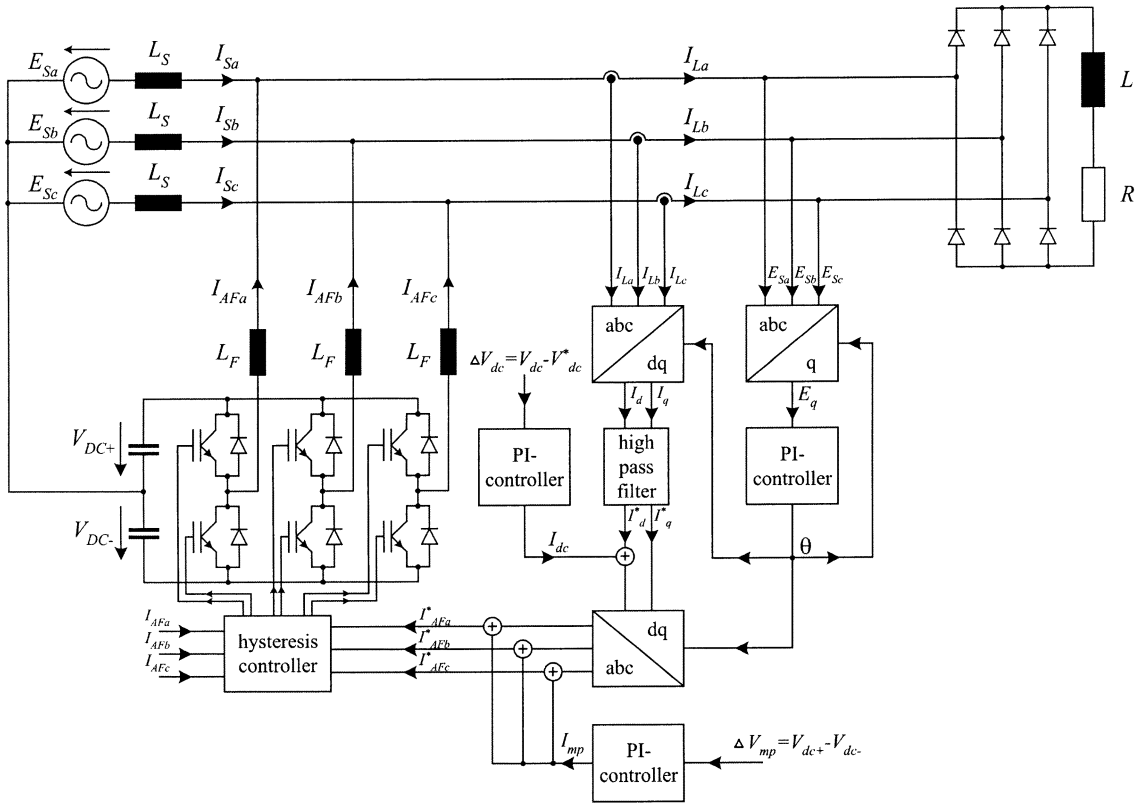

Fig. 8. Block diagram of the shunt active power filter.

The dq-signals of the load currents can be divided into dc-components and ac-components

$$\begin{aligned} I_{Ld} &= \widetilde{I}_{Ld} + \bar{I}_{Ld} \\ I_{Lq} &= \widetilde{I}_{Lq} + \bar{I}_{Lq} \end{aligned}.$$

The active dc-component $\bar{I}_{Ld}$ represents the positive sequence fundamental active power of the load currents, the reactive dc-component $\bar{I}_{Lq}$ represents the positive sequence fundamental of the reactive power of the load currents, and the ac-components $\widetilde{I}_{Ld}$ and $\widetilde{I}_{Lq}$ represent the total harmonic content of the load current.

The dq-components are high-pass filtered and the dc-components are subtracted to obtain the total harmonic content

$$\begin{aligned} I^*_{Ld} &= \widetilde{I}_{Ld} \\ I^*_{Lq} &= \widetilde{I}_{Lq} \end{aligned}.$$

The reference signals I^*_{AFa}, I^*_{AFb}, and I^*_{AFc} for the hysteresis controller are calculated by multiplying the dq-components I^*_{Ld} and I^*_{Lq} with the inverse transformation matrix

$$\begin{pmatrix} I^*_{AFa} \\ I^*_{AFb} \\ I^*_{AFc} \end{pmatrix} = \begin{pmatrix} \cos\Theta & \sin\Theta \\ \cos\left(\Theta - \frac{2\pi}{3}\right) & \sin\left(\Theta - \frac{2\pi}{3}\right) \\ \cos\left(\Theta + \frac{2\pi}{3}\right) & \sin\left(\Theta + \frac{2\pi}{3}\right) \end{pmatrix} \cdot \begin{pmatrix} I^*_{Ld} \\ I^*_{Lq} \end{pmatrix}.$$

C. Control of the Total dc Voltage

The dc link capacitor C_{dc} is fed by the ac system to which the APF is connected. The total dc voltage V_{dc} can be decreased by injecting active power from the dc capacitor into the system. Assuming a pure sinusoidal voltage supply, the current harmonics only add to the reactive power. Hence, the only active power that has to be injected by the power system into the dc link to maintain a constant dc voltage are the losses of the APF, primarily conduction and switching losses of IGBTs and diodes. So, if the total dc voltage V_{dc} is less than a reference value V^*_{dc}, active power has to be injected into the capacitor, i.e. the active power d-component of the current has to be reduced. The control of the dc voltage is realized with a digital PI-controller. The input of the controller is the dc voltage difference ΔV_{dc}

$$\Delta V_{dc} = V^*_{dc} - V_{dc}.$$

The output of the PI-controller I_{dc} is subtracted from the d-component of the current

$$I^*_{Ld} = \widetilde{I}_{Ld} - I_{dc}.$$

D. Controlling Symmetry of the dc Voltages

The dc link of the power converter has a midpoint connection, making it possible to inject three independent active filter currents. To assure the converter operates properly, the dc voltages V_{dc+} and V_{dc-} should be kept equal.

If the voltage V_{dc+} of the upper dc link capacitor is greater than the voltage of the lower capacitor $V_{dc-}(|V_{dc+}| > |V_{dc-}|)$ the voltage of the lower capacitor can be increased by injecting zero sequence filter currents into the power system. To realize this symmetrical division of the dc voltages a PI-controller is implemented. The input of the PI-controller is the difference ΔV_{mp} of both midpoint voltages V_{dc+} and V_{dc-}

$$\Delta V_{mp} = |V_{dc+}| - |V_{dc-}|.$$

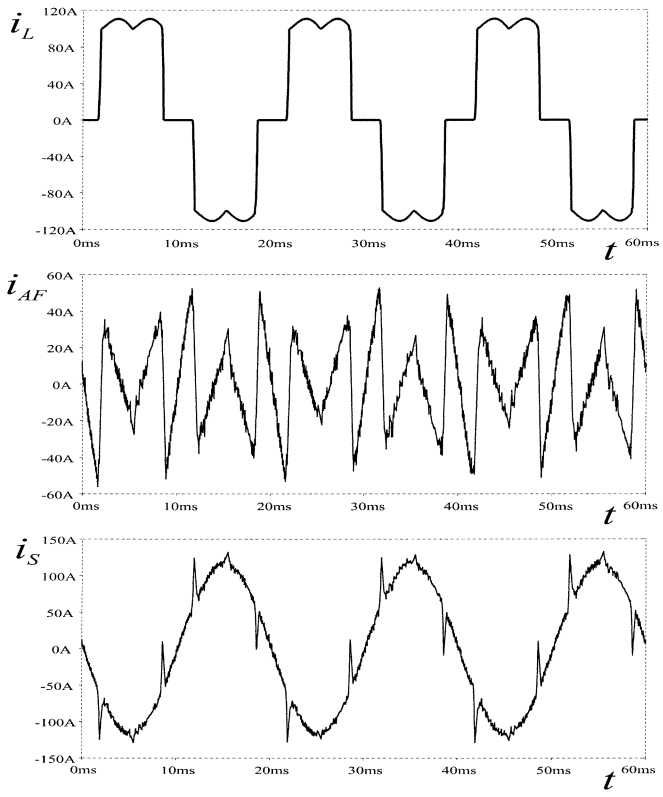

Fig. 9. Simulation results: load current $\mathrm{I_L}$, filter current $\mathrm{I_{AF}}$, and source current $\mathrm{I_S}$.

The output of the PI-controller I_{mp} is added to all three active filter currents

$$I^*_{AFa} = I^*_{AFa,old} + I_{mp}$$
$$I^*_{AFb} = I^*_{AFb,old} + I_{mp}$$
$$I^*_{AFc} = I^*_{AFc,old} + I_{mp}.$$

IV. Simulation Results

The shunt active power filter discussed in this paper has been investigated in the simulation environment PSpice, using the DSP model developed with the *Device Equations* option. This DSP model allows the digital regulator propagation delays and sampling times of a real digital system to be incorporated in the simulation without difficulties.

The harmonic load is simulated as depicted in Fig. 8. The load currents generated by the rectifier are square waved, 120° phase shifted. The resistance has a value of $R = 5\ \Omega$ and the inductance a value of $L = 2\ \mathrm{mH}$. The source inductance has a value of $L_S = 35\ \mu\mathrm{H}$ and a resistance of $R_S = 10\ \mathrm{m\Omega}$ in series. The source voltages are assumed to be sinusoidal. The total control as described in chapter III is implemented in the DSP model. The dc-link capacitance is $C_{dc} = 4.4\ \mathrm{mF}$.

Fig. 9 depicts the load current I_L, active filter current I_{AF}, and the source current I_S. The waveform of the source current is almost sinusoidal, only during the steep edges of the load currents the active filter is not able to track the current slopes.

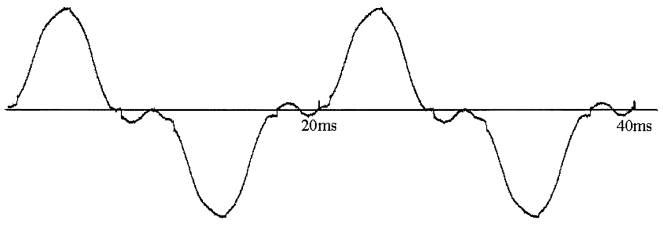

Fig. 10. Waveform of the phase voltage $\mathrm{E_S}$.

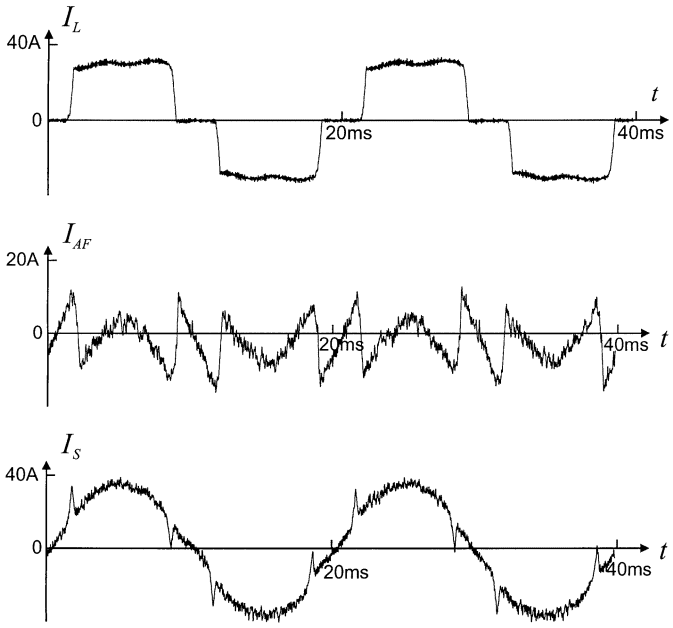

Fig. 11. Experimental result: load current $\mathrm{I_L}$, active filter current $\mathrm{I_{AF}}$, and source current $\mathrm{I_S}$.

V. Experimental Results

For the experimental results, control code developed above in PSpice is downloaded into the ISEADSP board. The harmonic load is a rectifier feeding a resistive-inductive load. The amplitude of the three source voltages was reduced using a Y-y-transformer. The typical waveform of the heavily distorted phase voltages is shown in Fig. 10.

The power part of the filter is created by two PEBBs. The midpoint connection of the dc-link is created by connecting two extra capacitors in series parallel to the PEBB capacitors C_{PEBB}, building a total capacitance of $C_{dc} = 4.44\ \mathrm{mF}$. The current smoothing inductances have a value of $L_F = 1.8\ \mathrm{mH}$.

The load current, active filter current, and the source current are depicted in Fig. 11. It is clearly shown that under these extreme circumstances the control of the shunt active filter is capable of calculating and compensating the harmonic content of the load current, even when the ac source voltages are heavily distorted (Fig. 10). These experimental results clearly verify the simulation results.

VI. Conclusion

In this paper, three rapid prototyping tools have been presented. A PSpice DSP model is developed to simulate the discrete behavior of digital processors, A/D-conversions, and D/A-

conversions. With this model, all kind of control algorithms can be thoroughly tested and investigated. The developed control algorithms can be downloaded into the real-time ISEADSP control board. The ISEADSP board is characterized by large computation power and large number of memory mapped input and output channels. The ISEADSP board can control a power converter created with power electronic building blocks (PEBBs). With these PEBBs different rectifier and inverter topologies can be built. The combined use of these three tools is very effective and improves productivity.

The power of these tools is demonstrated by developing a shunt active filter. Different control strategies have been tested in PSpice and were later used to implement in the ISEADSP board which controls the PEBB converter. The complete development and testing time was less then six man-months.

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Joep Jacobs (S'96) was born in The Netherlands in 1974. He received the M.S. degree in electrical engineering from Aachen University of Technology, Aachen, Germany, in 1999.

Since 2000, he has been a Research Associate at the Institute for Power Electronics and Electrical Drives (ISEA), Aachen. His current research interests are medium voltage dc–dc converters, VAR compensators, and harmonic power filters.

Mr. Jacobs received the IES Prize Paper Award.

Dirk Detjen (S'99) was born in Germany in 1971. He received the M.S. degree in electrical engineering from Aachen University, Aachen, Germany, in 1998.

Since 1998, he has been a Research Associate at the Institute for Power Electronics and Electrical Drives (ISEA), Aachen. His current research interests are harmonic power filters as well as simulation of high power semiconductors and power semiconductor technology.

Claus-Ulrich Karipidis was born in Germany in 1968. He received the Ph.D. degree in electrical engineering from the Aachen University of Technology, Aachen, Germany, in 2001.

He was a Research Associate at the Institute for Power Electronics and Electrical Drives (ISEA), Aachen, focussed on switched reluctance drives as well as versatile DSP and FPGA based digital hardware for control and real-time simulation applications. Since 2002, he has been a member of the Trains System Engineering Team, Siemens AG Transportation Systems.

Rik W. De Doncker (M'87–SM'99–F'01) received the Ph.D. degree (with highest honors) in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1986.

In 1987, he was appointed a Visiting Associate Professor at the University of Wisconsin, Madison, where he lectured and conducted research on field-oriented controllers for high-performance induction motor drives. In 1988, he was a General Electric Company Fellow in the Microelectronic Center, IMEC, Leuven. In December 1988, he joined the General Electric Company Corporate Research and Development Center, Schenectady, NY, where he led research on drives and high-power soft-switching converters, ranging from 100 kW to 4 MW, for aerospace, industrial, and traction applications. In 1994, he joined Silicon Power Corporation (formely GE-SPCO) as Vice President, Technology. He worked on high-power converter systems and MTO devices and was responsible for the development and production of a 15-kV medium-voltage transfer switch. Since October 1996, he has been a Professor at Aachen University, Aachen, Germany, where he leads the Institute for Power Electronics and Electrical Drives. He has published over 90 technical papers and is holder of 18 patents, with several pending.

Dr. De Doncker received two IAS Prize Paper Awards and is a member of the Verband der Elektrotechnik. He is the Past-Chairman of the Industrial Power Converter Committee of the IEEE Industry Applications Society and Vice-Chair of the IAS Industrial Power Conversion Systems Department. He is member of the IAS Executive Board, the Executive Committee of the IEEE Power Electronics Society, and the Executive Council of the EPE Association. He was founding Chairman of the German IEEE IAS-PELS Joint Chapter.